

ememory

**A Leading Logic NVM
Company**

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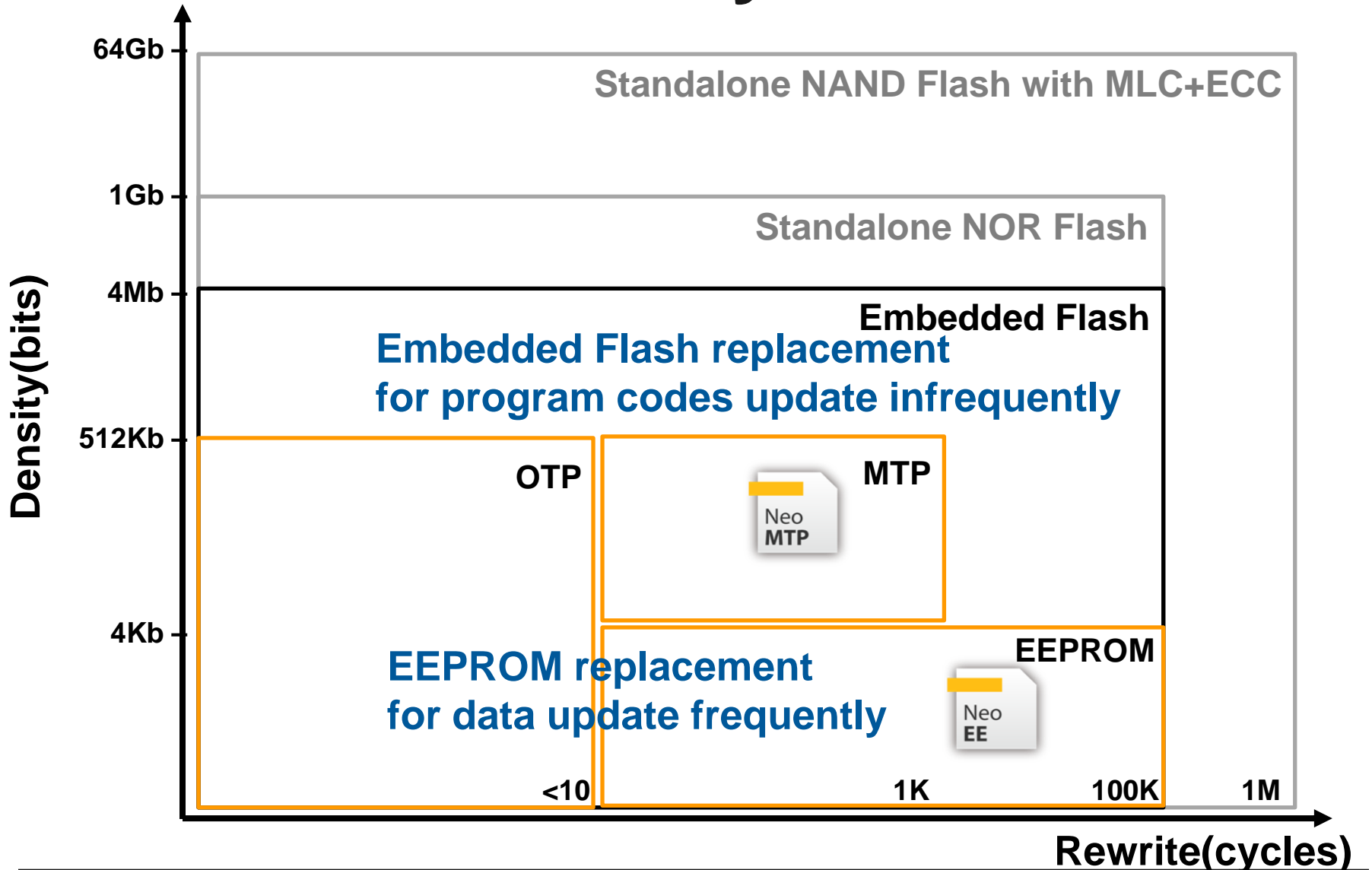
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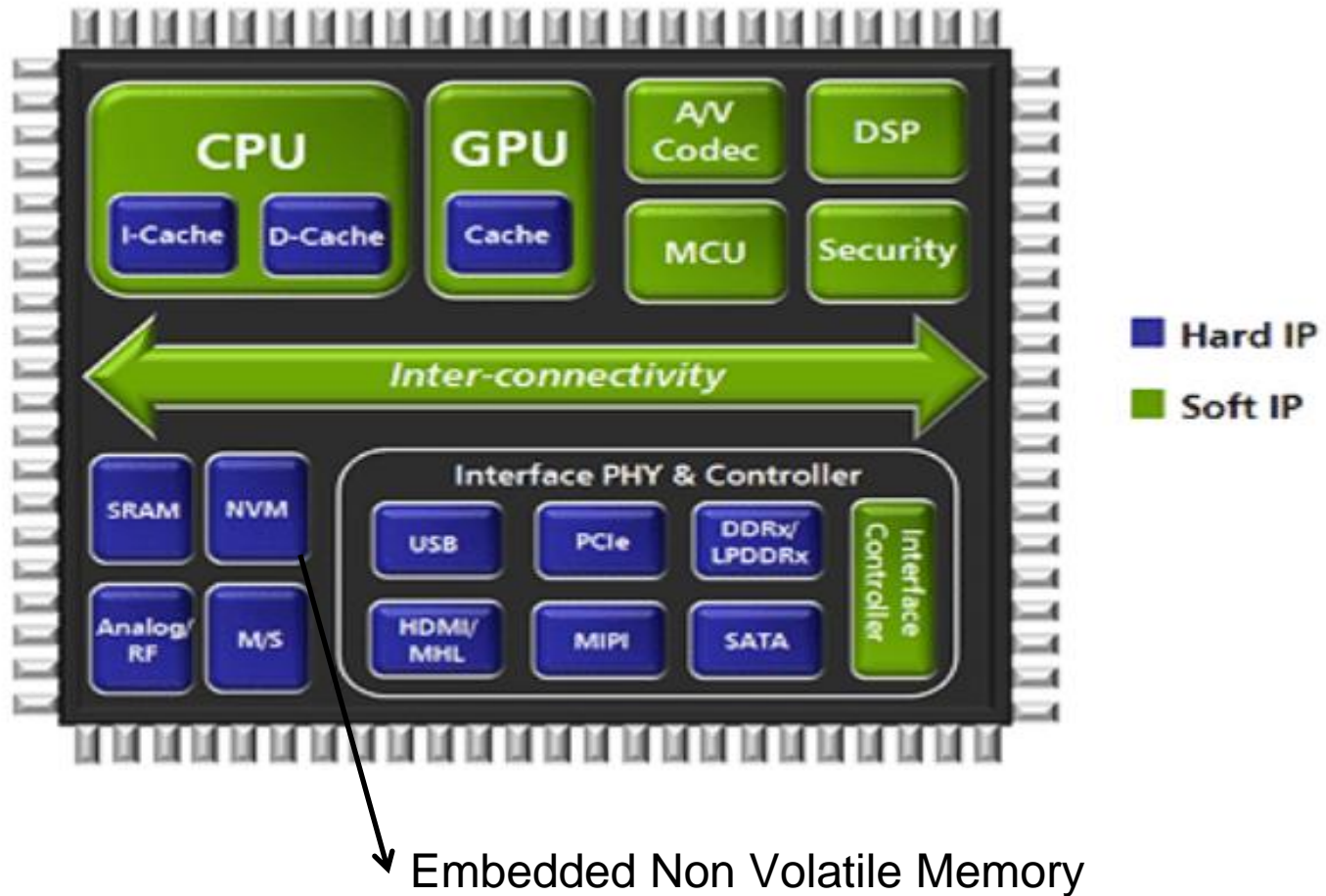
Outline

- **Business Model**
- **Review of Operations**
- **Growth Opportunity and Future Outlook**
- **Q & A**

Nonvolatile Memory Classifications



SOC Block Diagram



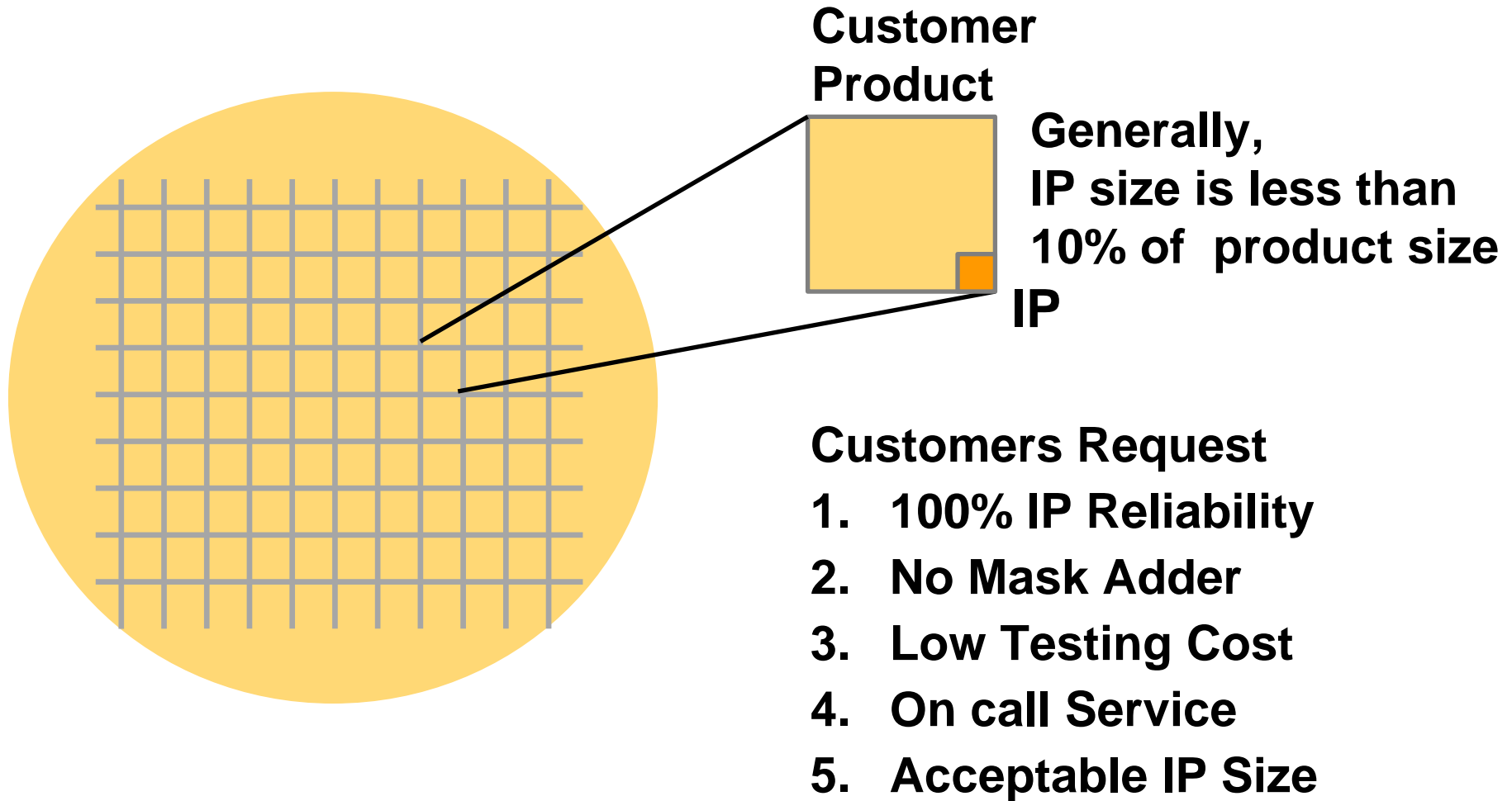
Source : tsmc

Embedded NVM Technologies

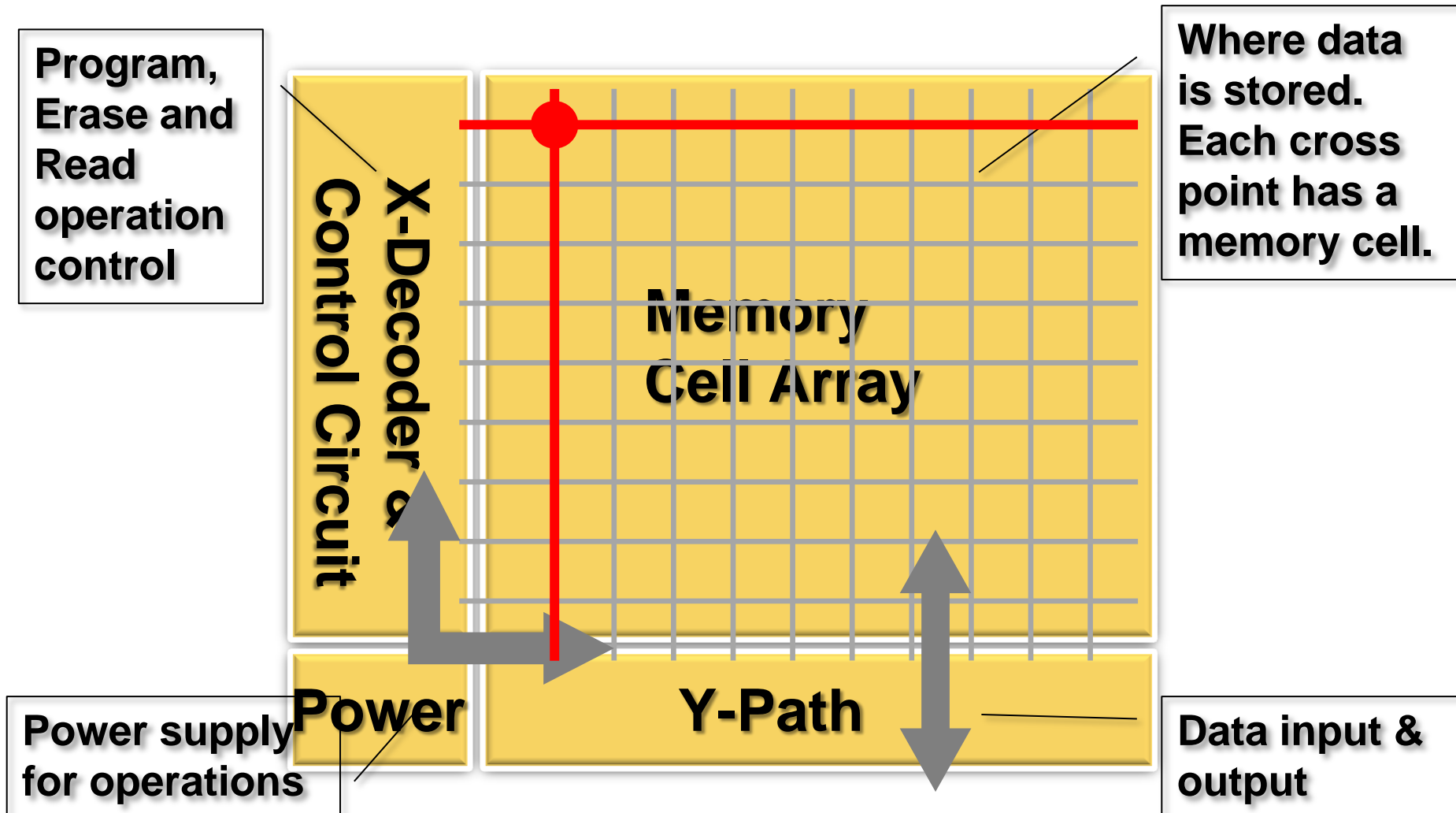
	ROM	eFuse (OTP)	Antifuse (OTP)	CMOS Floating Gate (OTP)	CMOS Floating Gate (MTP)	Embedded Flash
Cell Structure	Transistor	Poly Fuse	Antifuse	Floating Gate	Floating Gate	Floating Gate
Standard CMOS Compatible	Yes	Yes	Yes	Yes	Yes	No
Bitcell Area	< 1	50	1	2	4	1
Endurance	No	No	< 10	< 10	10K-100K	100-1000K
Density	4Kb-1Mb	256bit-4Kb	16bit-1Mb	16Kb-1Mb	1Kb-2M	64Kb-4Mb
Security	Low	Low	High	High	High	High
Additional Steps	None	None	None	None	None	+10 Mask

- ROM not programmable, eFuse cannot scale beyond 16Kb, embedded flash expensive and cannot scale after 40 nm
- eMemory's IPs: OTP (antifuse, floating gate) and MTP (floating gate)

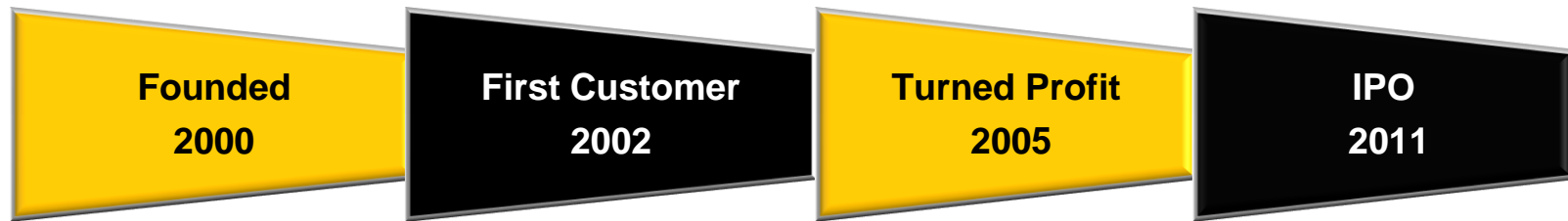
Considerations for IP Adoption



Inside Nonvolatile Memory IP



About eMemory



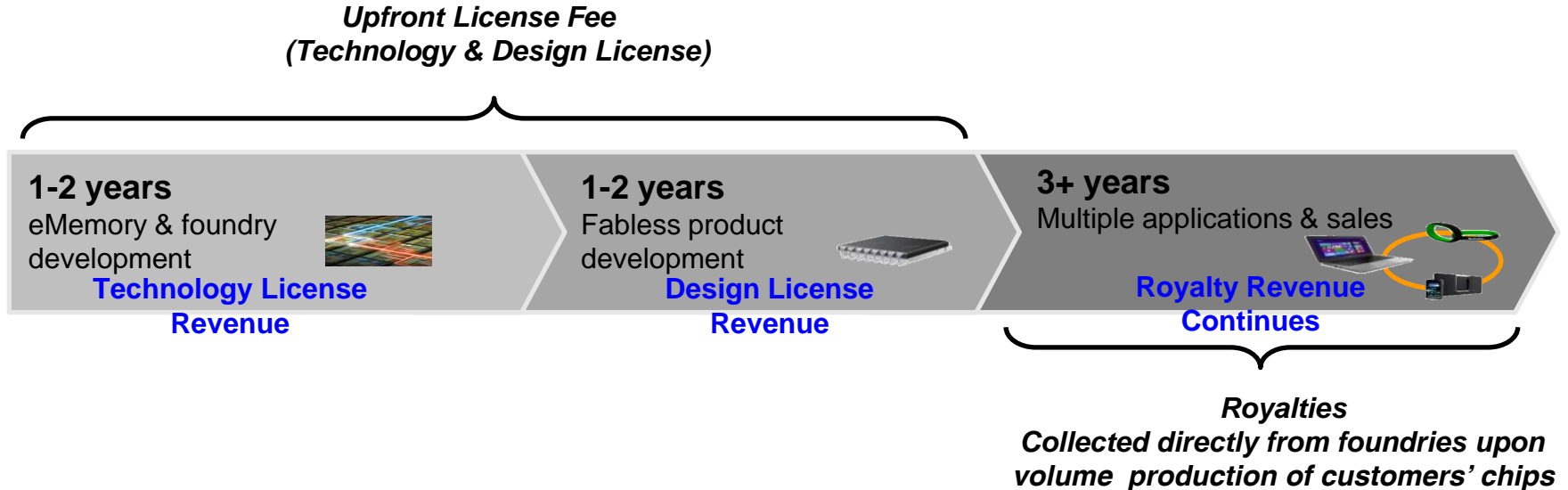
- Largest Logic Non-Volatile Memory (NVM) IP company
- 238 employees (166 R&D)*.
- No fundraising from capital markets or bank loans since IPO in 2011.
- Over 90% of earnings distributed in cash dividends.

Note*: As of Sep. 30th, 2017

Business Model

- Growth Metrics

- › No. of Embedded Platforms
- › No. of Design Licenses
- › Royalty



Worldwide Customers



Foundry



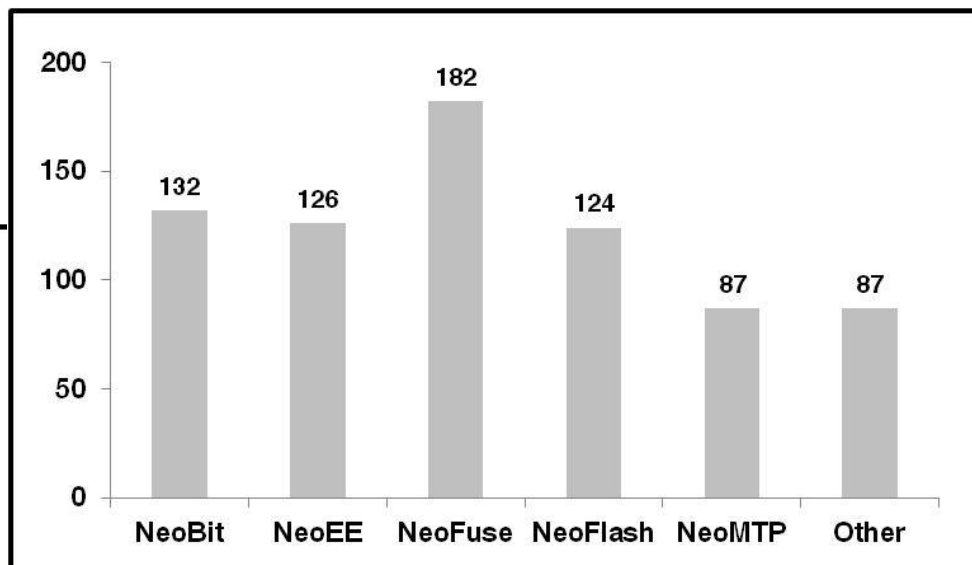
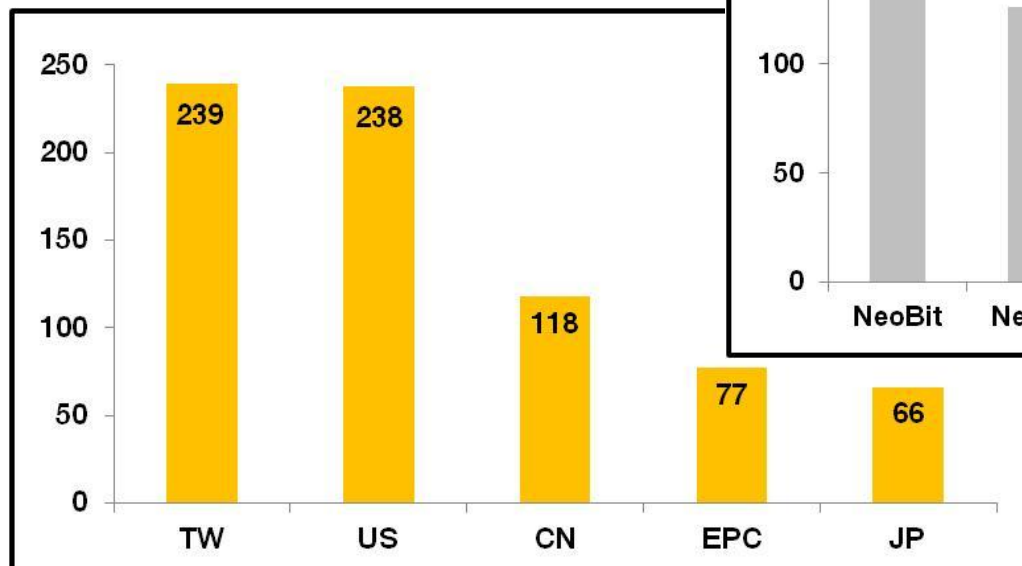
IDM



	Taiwan	China	Korea	Japan	North America	Europe	Others
Foundry	5	8	3	4	1	2	1
IDM	0	0	0	8	2	1	0
Fabless	261	513	71	52	242	111	53

Patent Portfolio

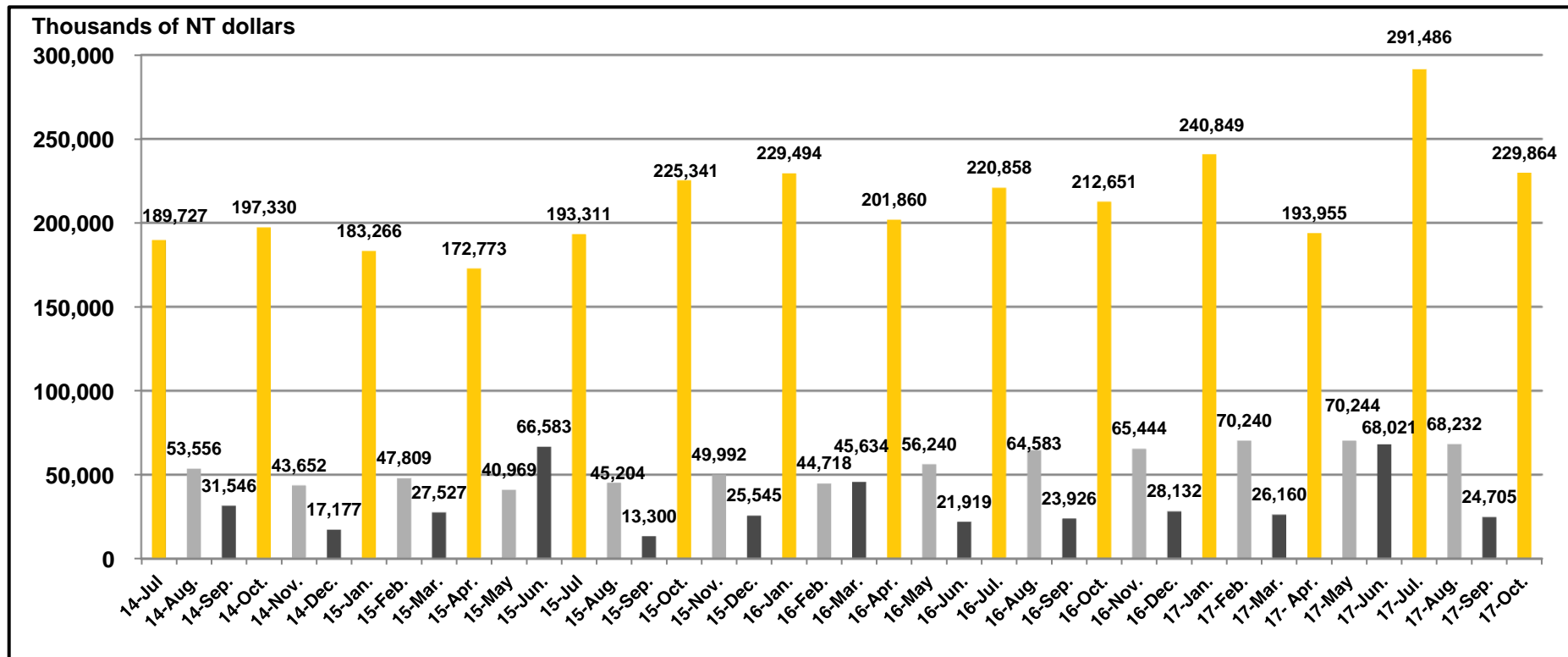
	2Q 17	3Q 17	Change
Pending	232	252	+ 20
Issued	453	486	+ 33
Total	685	738	+ 53



Note: As of Sep. 30th, 2017

Quarterly Revenue Pattern

- 1st month: Receive **License Fees** of the month and **Royalty** from most foundries on previous quarter's wafer shipments
- 2nd month: Receive **License Fees** of the month and **Royalty** from other foundries
- 3rd month: **License Fees** Only.



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Q3 Revenue Breakdown

Thousands of NT dollars

K NTD	Q3 2017	Q2 2017	QoQ	Q3 2016	YoY	Q1 – Q3 2017	Q1 – Q3 2016	YoY
Licensing	101,087	134,140	-24.6%	86,712	16.6%	309,373	250,403	23.6%
Royalty	283,336	198,080	43.0%	222,655	27.3%	744,519	658,829	13.0%
Total	384,423	332,220	15.7%	309,367	24.3%	1,053,892	909,232	15.9%

Number of Licenses

		Q3 2017	Q2 2017	2016	2015
Technology Licenses		4	8	43	28
Design Licenses	NRE	23	13	56	57
	Usage	87	77	311	349

Financial Income Statement

Amount in Thousands of NT Dollars, except margins/EPS/ROE

	Q3 2017	Q2 2017	Q3 2016	change (QoQ)	change (YoY)
Revenue	384,423	332,220	309,367	15.7%	24.3%
Gross Margin	100%	100%	100%	-	-
Operating Expenses	205,291	188,562	173,605	8.9%	18.3%
Operating Margin	46.6%	43.2%	43.9%	3.4ppts	2.7ppts
Net Income	194,062	135,610	130,299	43.1%	48.9%
Net Margin	50.5%	40.8%	42.1%	9.7ppts	8.4ppts
EPS	2.56	1.79	1.72	43.0%	48.8%
ROE	40.2%	29.6%	28.9%	10.6ppts	11.3ppts

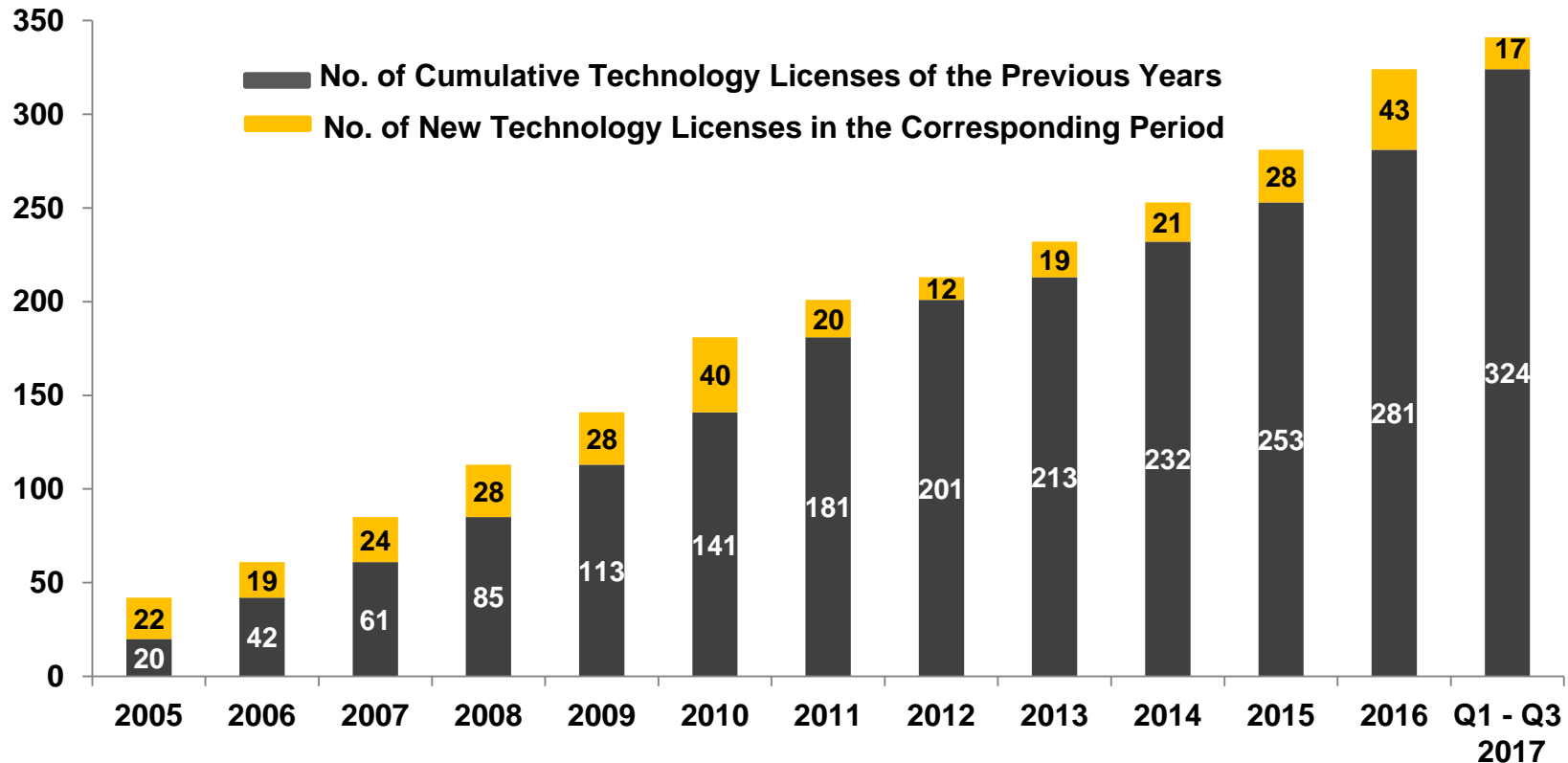
Note : Revenue amount in US dollars, QoQ growth of 15.5% and YoY growth of 30.4%.

Technology Licensing

Number of Licenses

Year	2014	2015	2016	Q1- Q3 2017
License	21	28	43	17

Note: Terms (including number of process platforms and licensing fees) for each technology license are set contractually. Payments are made according to set milestones, and there are no particular seasonal factors involved.



New Technologies Under Development

- New technologies being developed for **108** platforms by Q3 17.
- **21** for NeoBit, **42** for NeoFuse, **19** for NeoEE, and **26** for NeoMTP.

	7/10nm	12/14/16nm	28nm	40nm	55/65nm	80/90nm	0.11~ 0.13um	0.15~ 0.18um	>0.25 um
NeoBit	-	-	-	-	-	-	9	12	-
NeoFuse	3	3	7	5	10	7	3	4	-
NeoEE	-	-	-	-	-	-	2	17	-
NeoMTP	-	-	-	1	1	2	7	15	-

Note: As for Sep. 30th, 2017

Technology Developments by Processes

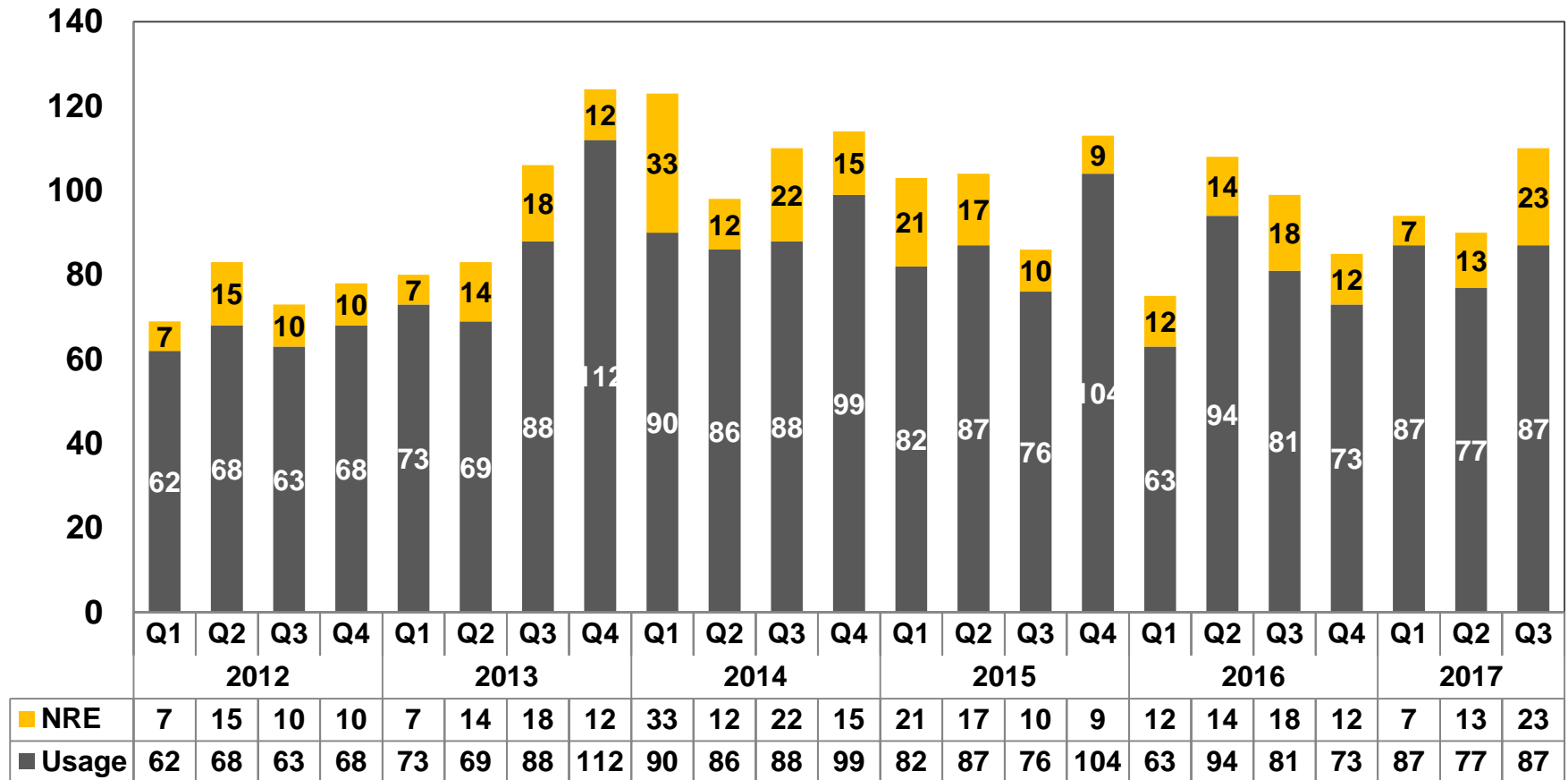
12" Fabs	Production	Development	NVM Type	Process Type
7/10nm	0	3	OTP	FF
12/14/16nm	2	3	OTP	FF+
28nm	9	7	OTP	LP/HPM, HLP/HPM, LPS
40nm	8	6	OTP, MTP	HV-DDI, LP, eFlash
55/65nm	14	11	OTP, MTP	LP, HV-DDI, HV-OLED, DRAM, CIS, eFlash
80/90nm	6	6	OTP, MTP	HV-DDI, HV-OLED, LP, eFlash
0.13/0.11um	9	1	OTP, MTP	HV-DDI, BCD, Generic
0.18um	1	0	OTP	BCD
Total	49	37		

8" Fabs	Development	NVM Type	Process Type
90nm	3	OTP	HV-DDI, LL
0.13/0.11um	20	OTP, MTP	HV-DDI, BCD, LP, RF, CIS, LL, Green
0.18/0.16/0.152um	48	OTP, MTP	Generic, LP, LL, MR, HV, Green, BCD
0.25um	0	OTP, MTP	BCD
0.35um	0	OTP	UHV
Total	71		

Note: As of Sep. 30th, 2017

Design Licensing (New Tape-Out)

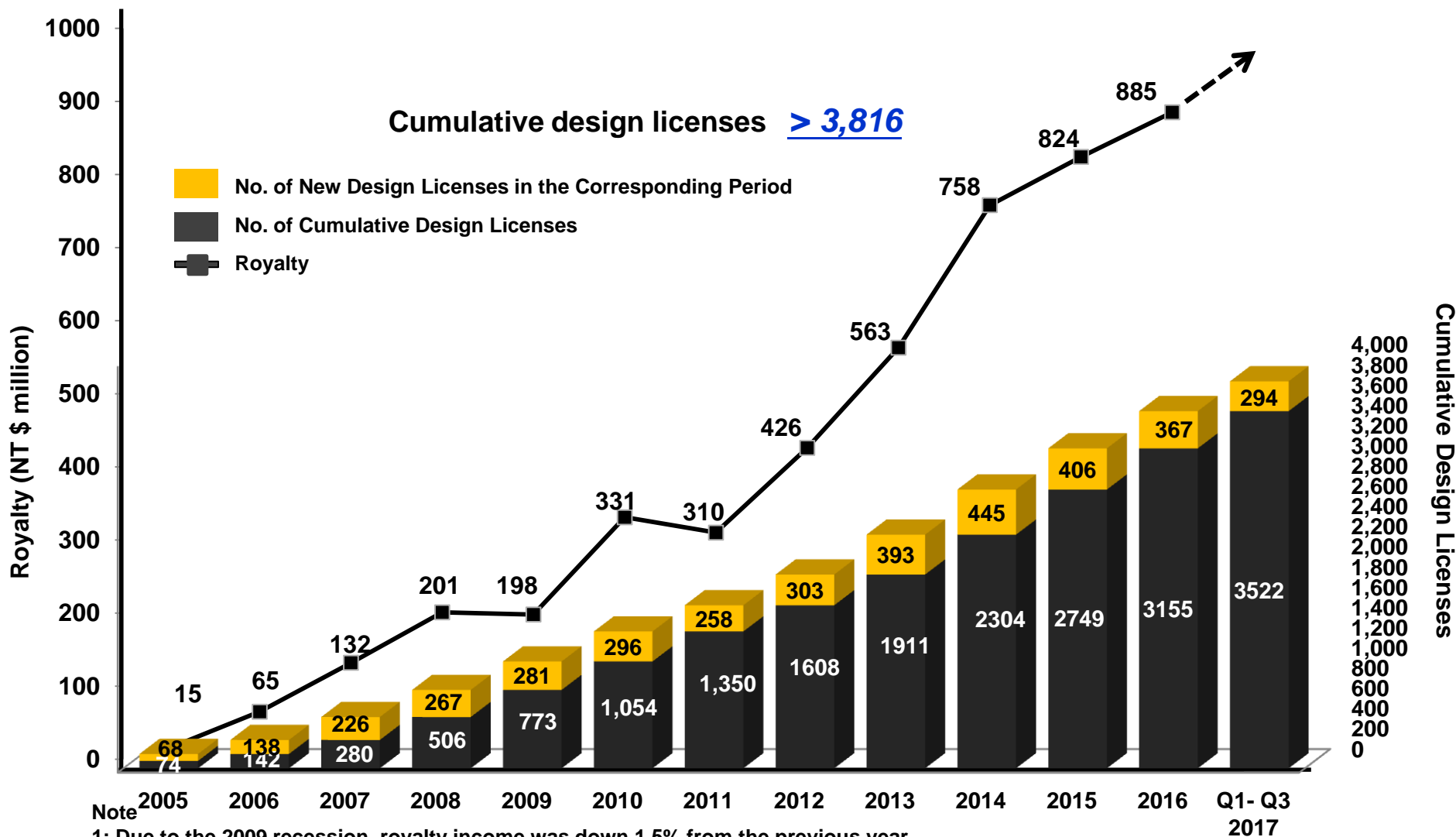
- A total **294** NTO in Q1-Q3 2017 (**367**@2016, **406**@2015, **445**@2014, **393**@2013)



Note*: As the applications of MCU at several foundries have gradually entered mass production, and the business model of the main foundry partner which provides green process has shifted to — eMemory licenses IP cell to the foundry for it to provide direct design service to customers — as the result, the new tape out number of MCU has been affected, but the royalty coming from IP cell usage continues to roll in.

In summary, even the new tape out number of MCU is lower than before; the corresponding wafer output and royalty continue to grow.

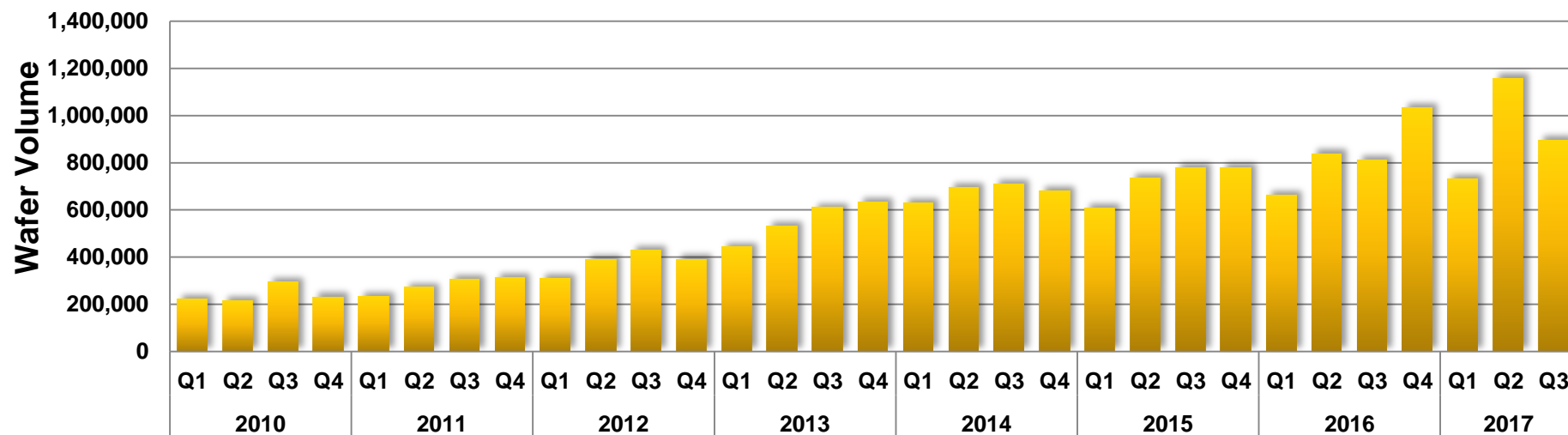
Cumulative Licenses Drive Future Royalties



Note

- 1: Due to the 2009 recession, royalty income was down 1.5% from the previous year.
- 2: Prepaid royalty from a single customer contributed to 2010 annual growth of 67%, followed by a drop of 6.3% in 2011.
- 3: CAGR for 2009-2013 was 30%.

Wafer Production Volume



eMemory IP's Penetration Rates in T Company (in US \$ revenue)

	Process node	*% of T	Q3 17	Q2 17	2016	2015
8"	0.25/0.35	2%	34.06%	44.84%	28.15%	33.49%
	0.15/0.16/0.18	10%	7.93%	7.36%	12.43%	8.73%
	0.11/0.13	3%	55.97%	58.76%	42.61%	29%
12"	80/90nm	5%	13.88%	12.73%	12.50%	19.85%
	55/65nm	10%	2.22%	4.73%	3.59%	0.55%
	40/45nm	12%	0.12%	0%	0%	0%
	28nm	23%	0.01%	0.18%	0.55%	0.05%
	16/20nm	24%	0%	0%	0%	0%
	10nm	10%	0%	0%	-	-
8"		16%	20.34%	21.77%	18.86%	16.64%
12"		84%	1.13%	1.43%	1.44%	1.87%
Total		100%	4.20%	5.07%	4.27%	4.76%

* T company's Q3 2017 revenues broken down by process nodes, the royalty was recognized in eMemory's Oct. revenue.

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eMemory's NVM Technologies

- **Logic NVM portfolio offers one-stop-shop solution.**

- › Compatible to any process
- › Robust structure
- › Low process cost
- › Competitive macro sizes
- › Easy integration
- › Easy porting

eMemory's NVM Technology	OTP			MTP	
	NeoBit	NeoFuse	NeoFlash	NeoEE	NeoMTP
Product Type	OTP	OTP	Flash	EEPROM	MTP
Endurance (Cycles)	10	10	1K~10K	10K~100K	1K~10K
Additional Mask Steps	0	0	2-3	0	0
Technology	Floating gate	Anti-Fuse	SONOS	Floating gate	Floating gate
Scalability	Simple	Simple	Simple	Simple	Simple
Memory Density	HD < 512Kb GHD < 16Mb	< 4Mb	< 2Mb	< 4Kb	< 512Kb

Applications by Technology

12"						8"				
7nm	10nm	12/14/16nm	28nm	40nm	55/65nm	80/90nm	110/130nm	160/180nm	250nm	350nm

NeoBit



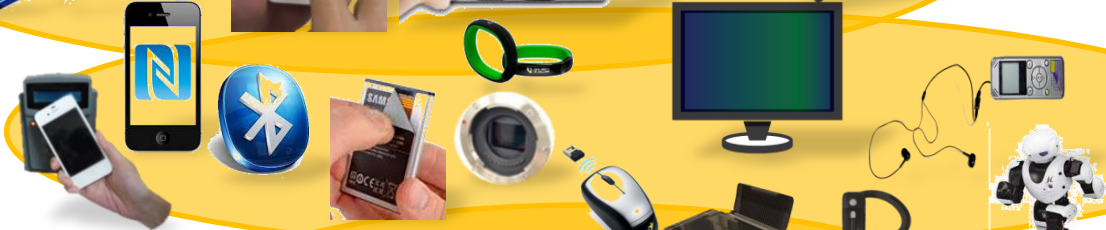
NeoFuse



NeoFlash



NeoEE

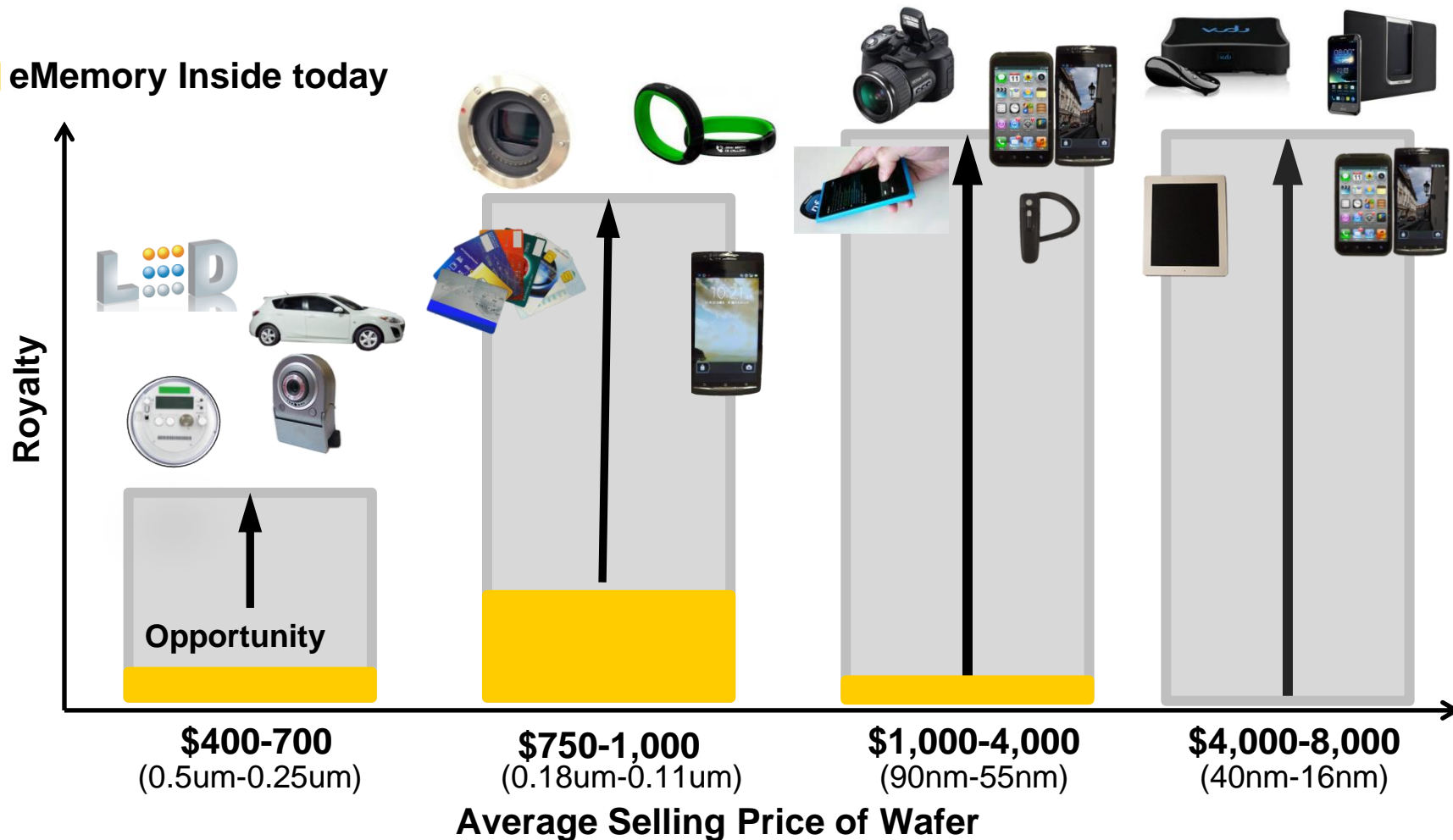


NeoMTP



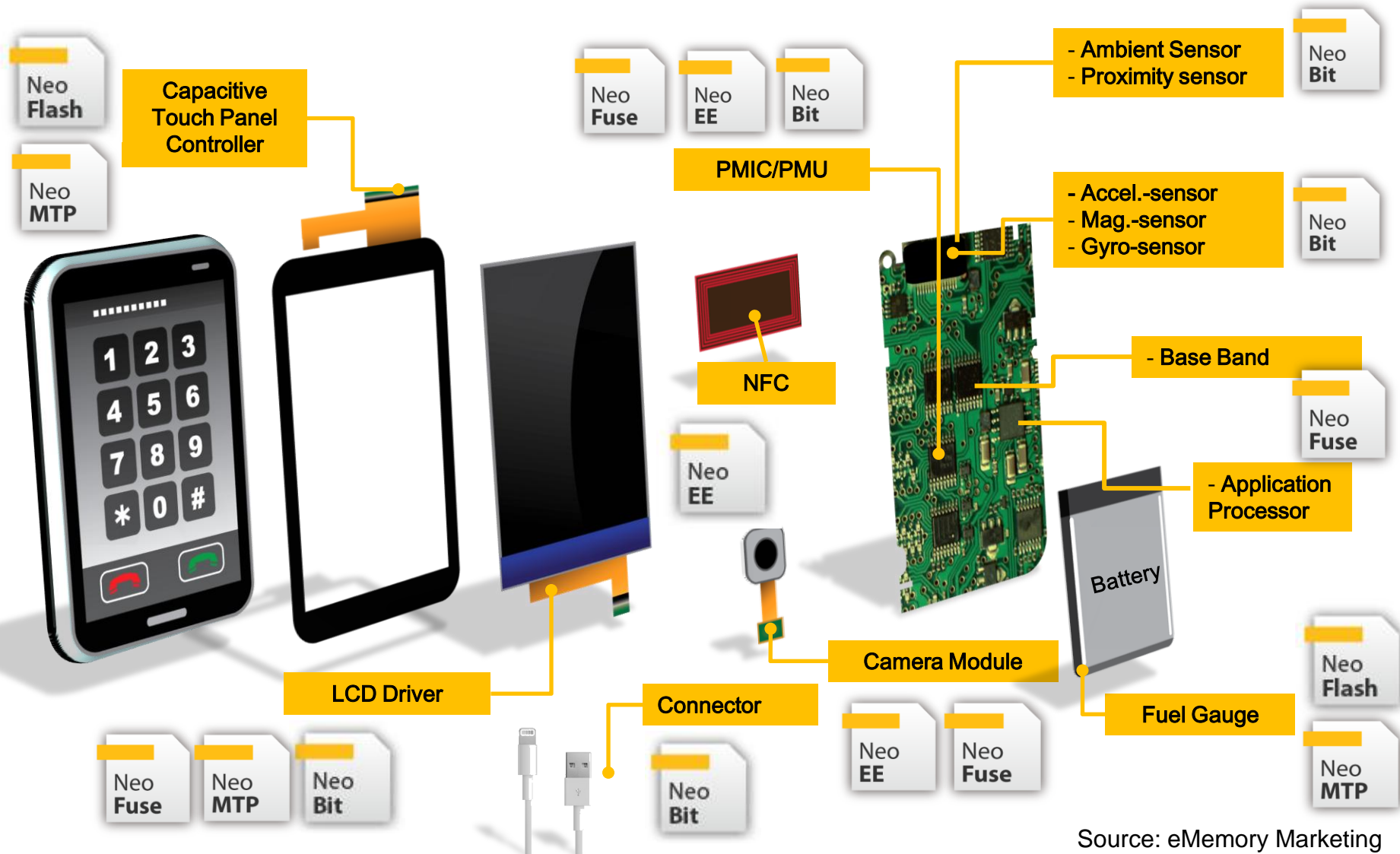
Opportunity at all Price Points

 eMemory Inside today



Note: 2.2 million 8" equivalent wafers with eMemory IP were shipped in 2013. (~5% of WW foundry shipment)

eMemory IP in Smart Phone



Source: eMemory Marketing

Benefits from Using eMemory IPs

Design-in for

1. Trimming
2. Parameter Setting
3. Code Storage
4. Identification Setting
5. Encryption
6. Function Selection

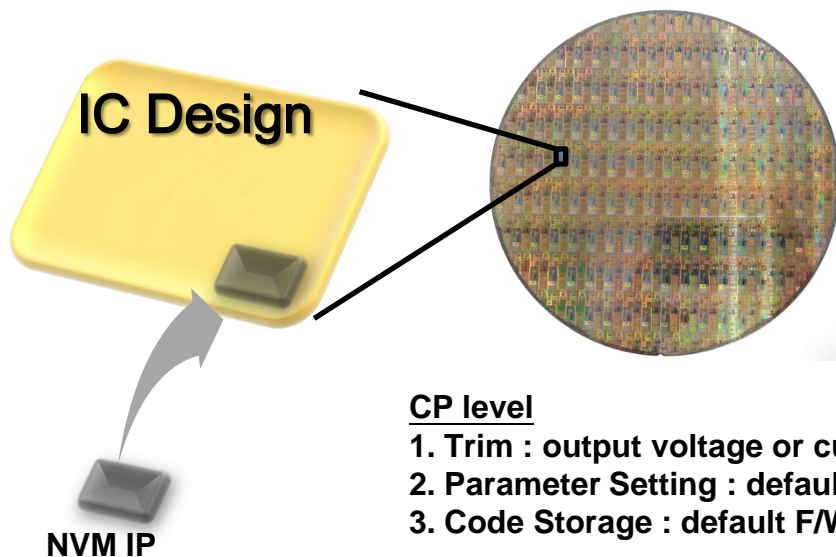
Package/FT level

1. Trim : SPEC shift
2. Parameter Setting : cross chip optimization
3. Identification Setting : manufacturer resume
4. Function Selection : setting for target market

CP Test

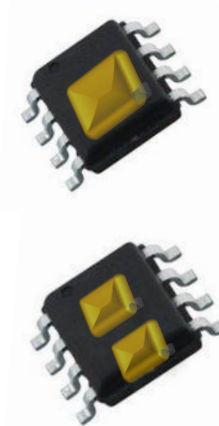
Package/FT

System Assembling



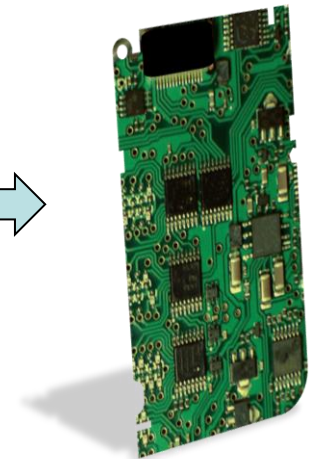
CP level

1. Trim : output voltage or current
2. Parameter Setting : default value
3. Code Storage : default F/W code



System Assembling

1. Parameter Setting : cross chip optimization
2. Code Storage : F/W code modification
3. Identification Setting : manufacturer resume
4. Encryption : Security algorithm or key storage



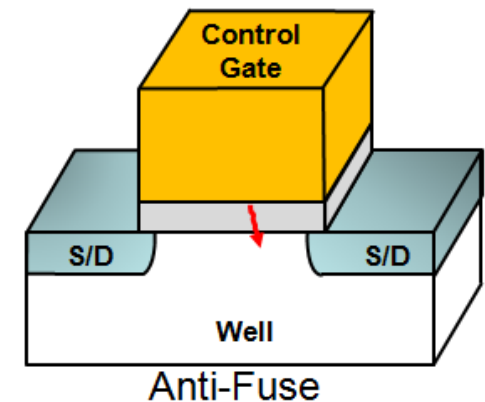
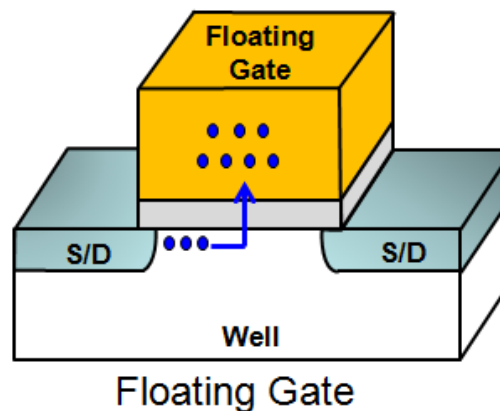
Invisibility for Security

- Provide “Invisible Hardware Key” for invisible storage
- Prevent reverse-engineering to detect content of security key
- Protect firmware and hardware of ICs from pirating
- Extend & protect customer’s business

eFuse Key: Data is easily observed



Invisible Hardware Key : Data is hard to be detected



Security & Protection

Authorized Product



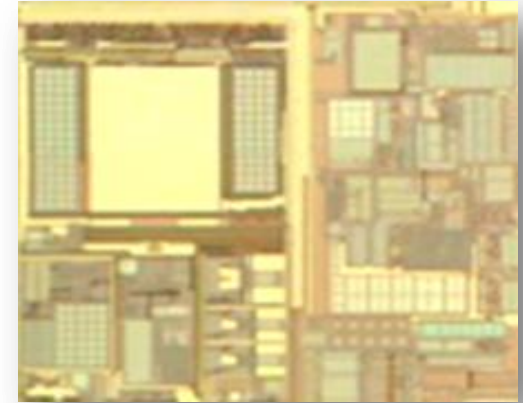
reverse
copy

re-produce



without protection

Fake Product

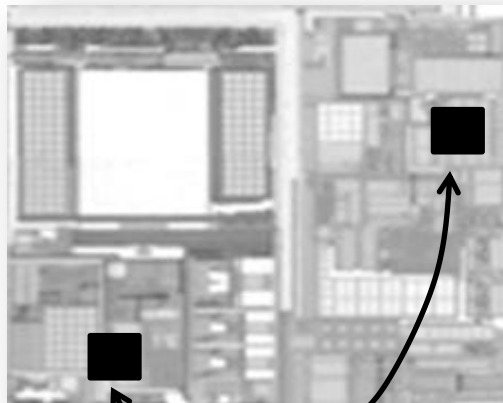


reverse
copy

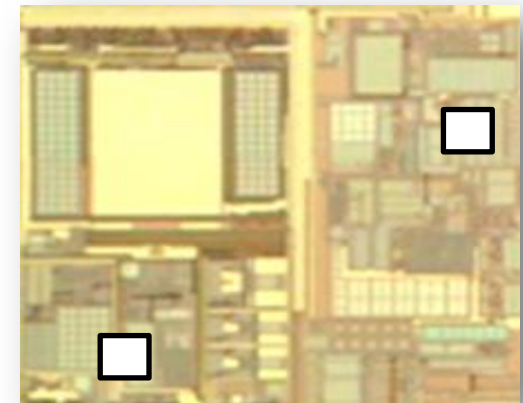
re-produce



with protection

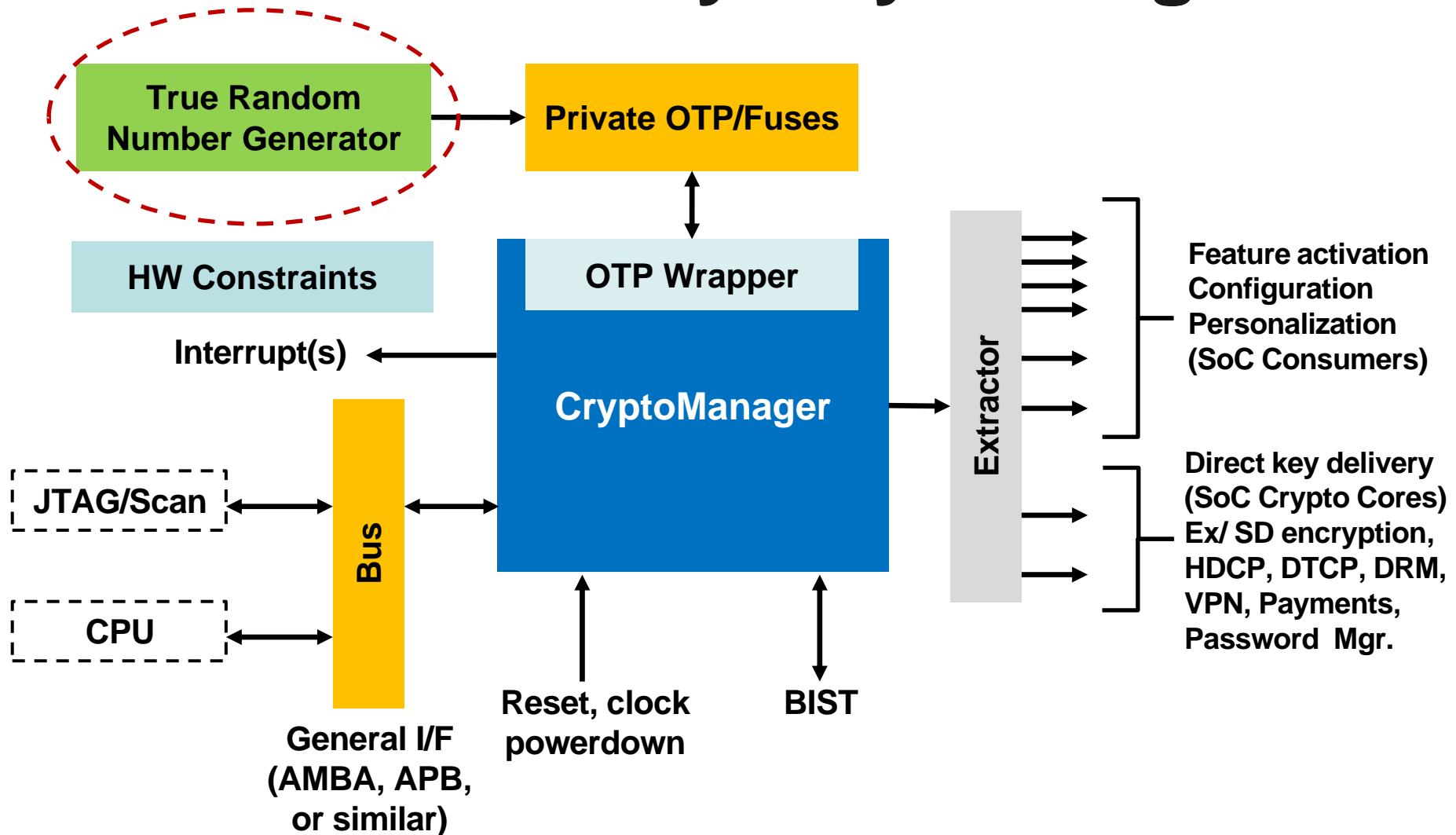


Security IP/Code by
Authorized Use



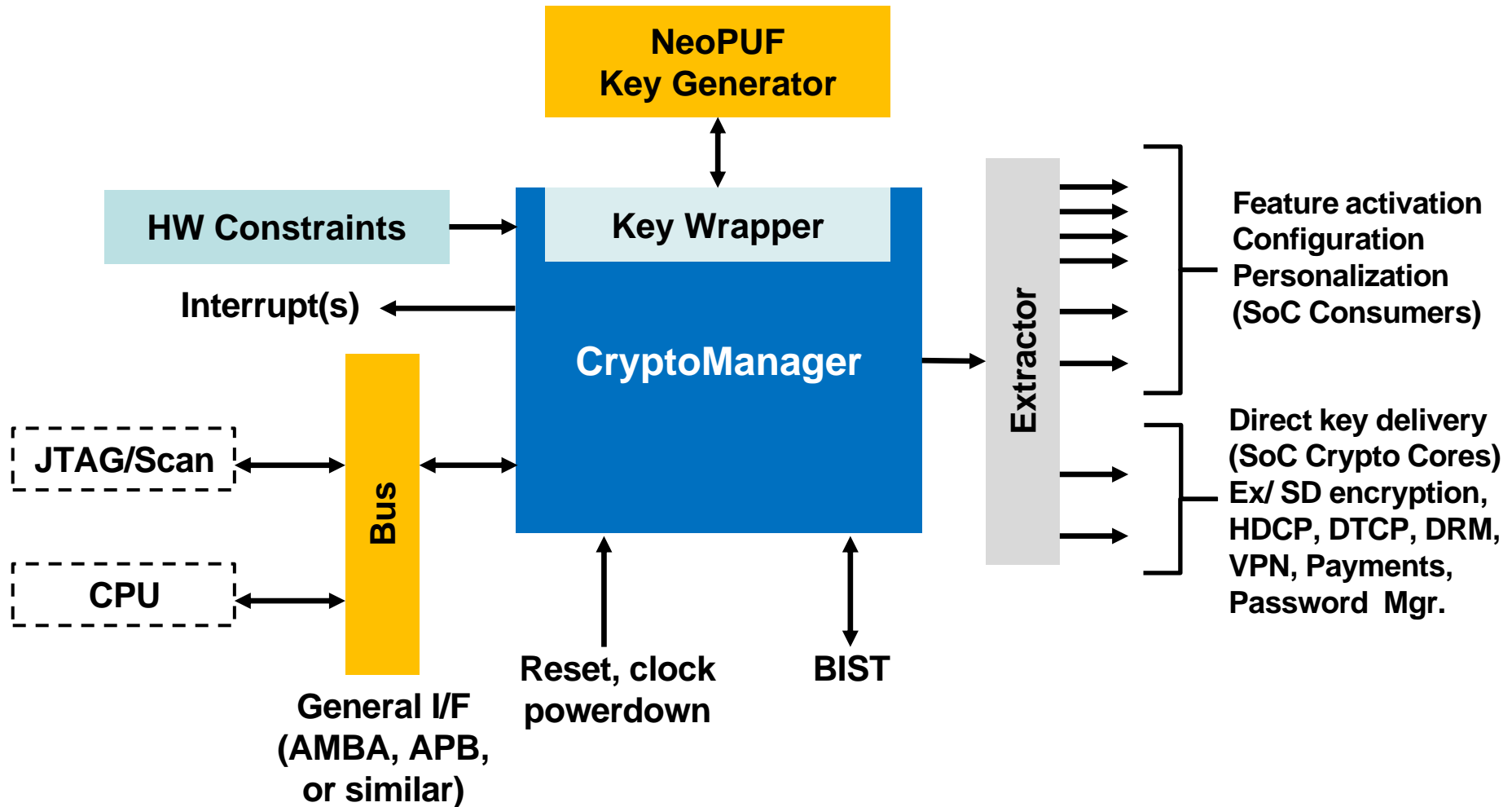
Can NOT Work w/o
Security IP/Code

OTP for security Key storage



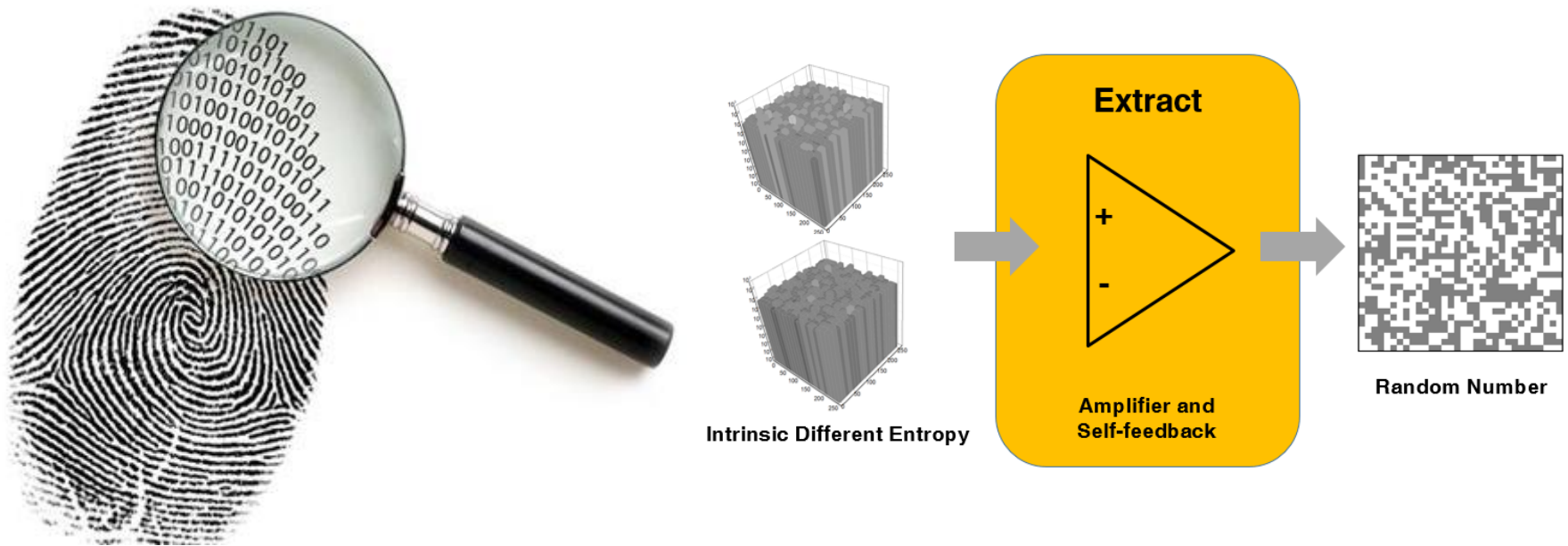
Source : Rambus crypto manager platform

NeoPUF for Security Key Generation



Source : Rambus crypto manager platform

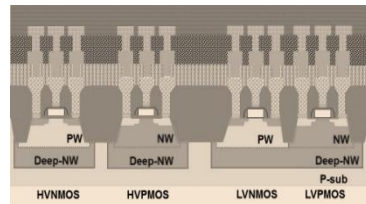
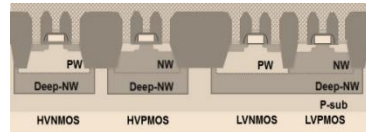
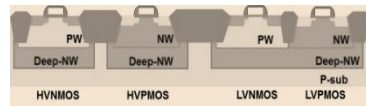
What is P_{hysical} U_{nclonable} F_{unctions}



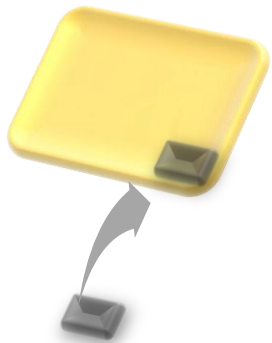
Collision Probability $\doteq 1/15B \doteq 1/2^{34}$ Collision Probability = $1/2^{\text{Bits Stream Length}}$

NeoPUF Technology

Wafer Process



IC Design

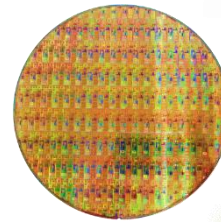


eMemory IP

Design-in
Customized SPEC & Function are designed for customer demands

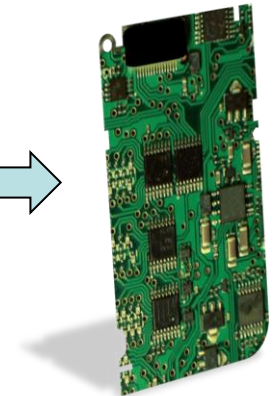
Manufacturing
Process Variation is introduced during manufacturing process (+0 mask logic process)

CP /FT Test



Product Testing
Random Noise is enhanced and generated randomly

System Assembling



System Assembling
Random Seed activates Identification, Encryption, Authentication, Security Key Storage

NeoPUF - Essential Security Component

- **Unique & unclonable hardware root of trust**
- **Authentic random number generator**
- **Every chip equipped with its own “fingerprint”**
- **Multiple functions:**
 - › **Encryption-decryption key to secure stored data**
 - › **Public-Private key pair generation**
 - › **Digital signature of hardware**
 - › **Device secure booting**

NeoPUF – Authentication & Security Everywhere



Smart Payment/IoT Device/Data Center

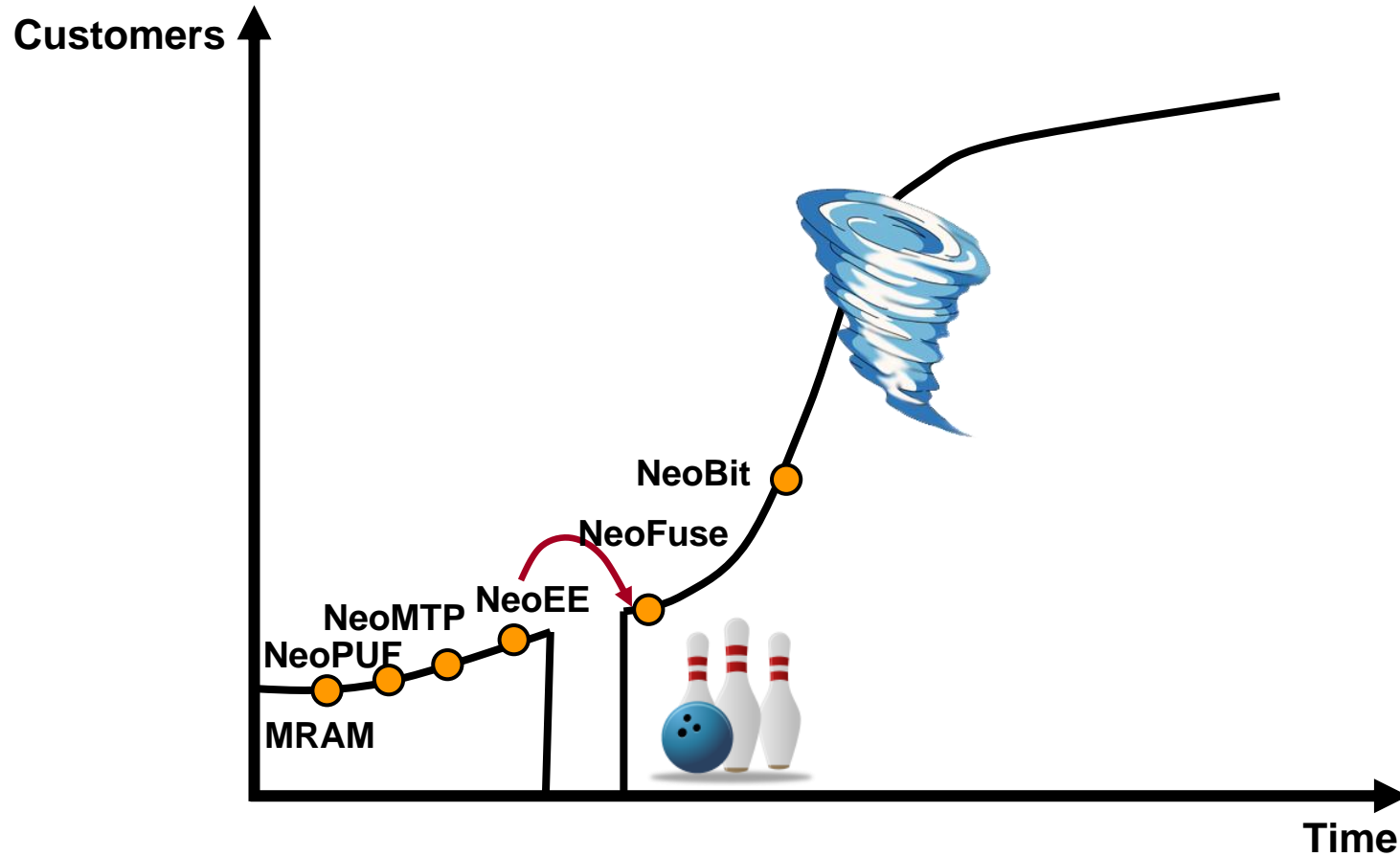


Data Storage Security



Hardware ID Tracking

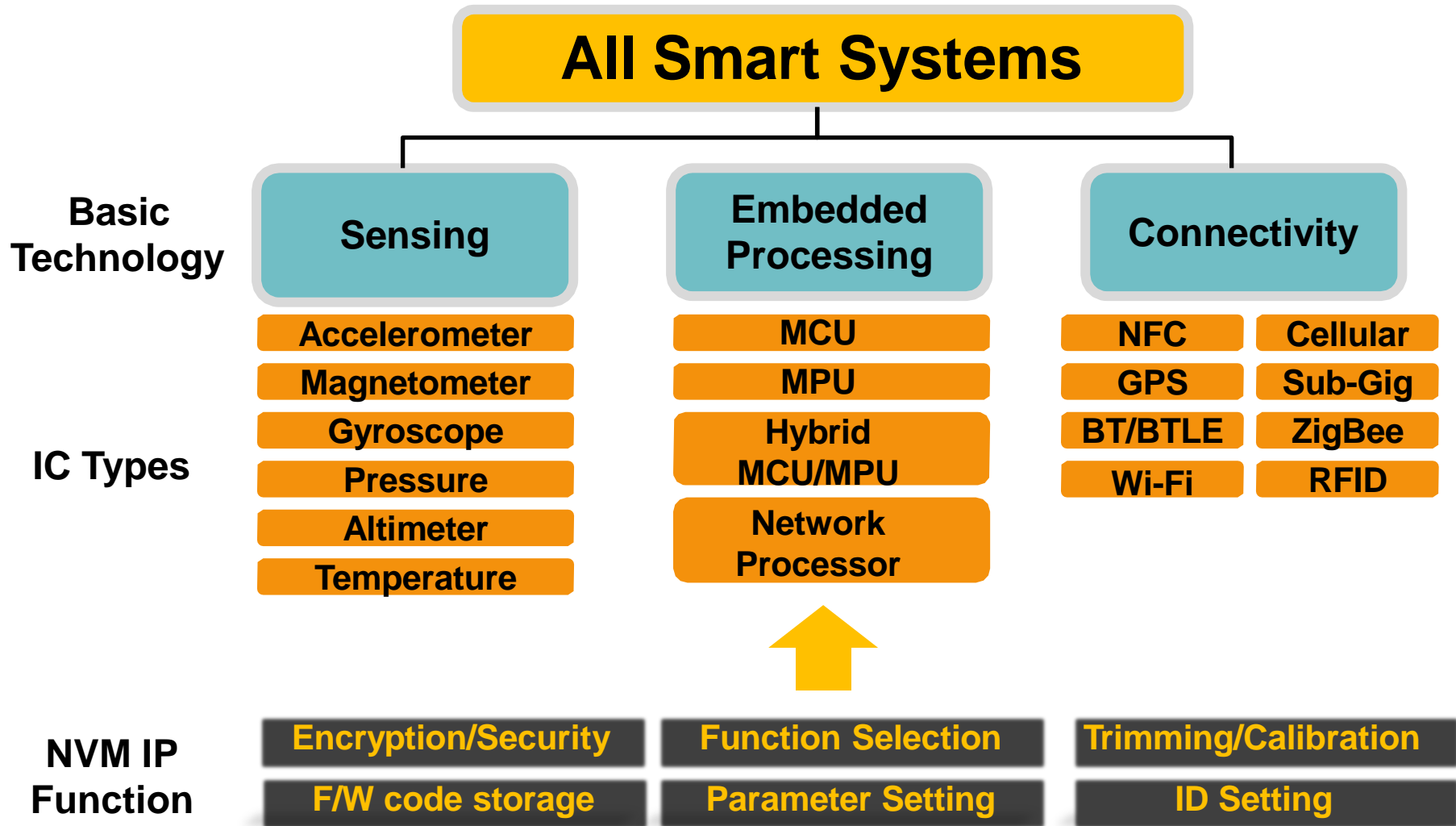
Crossing the Chasm



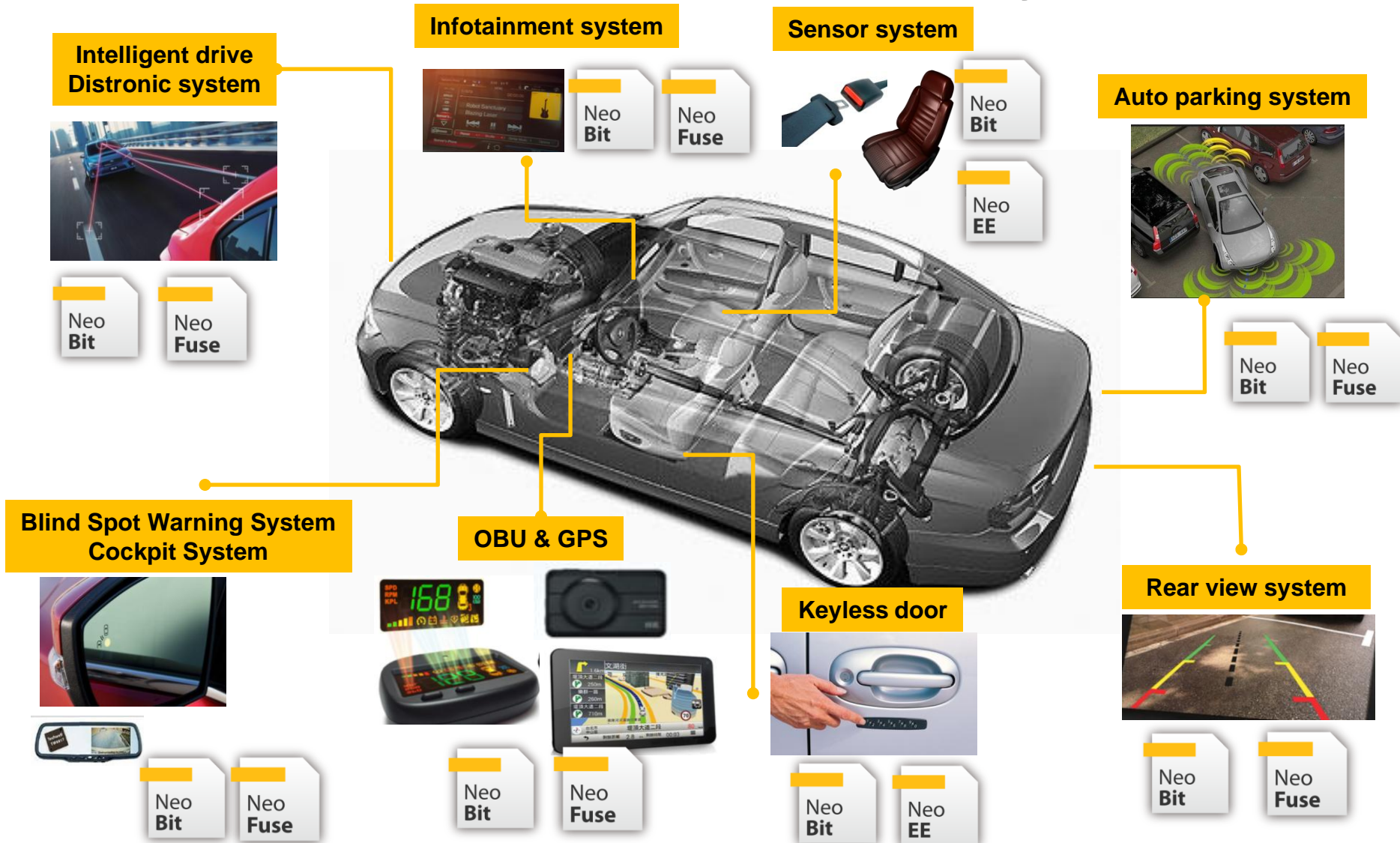
Security with eMemory IPs



NVM IP Demand in IoT



Autotronics with eMemory IPs



Outlook for Q4 and beyond

- **Key drivers to licensing revenue:**

- We are establishing partnerships with more foundries worldwide on various process nodes.
- Our growing IP library will boost design license revenue.

- **Key drivers to royalty revenue :**

- 8-inch processes**

- **PMIC royalty is to pick up strongly with content increase in new smartphones, such as Type C and Wireless Charger. This segment will also grow on the change of business terms with US largest chipmaker from one-time fee to royalty-based.**
 - **Our MTP has been adopted by a European IDM and ready for production.**

Outlook for Q4 and beyond

- Face ID related IC has been taped out in the third quarter.
- Automotive customers have started volume production this year.

12-inch processes

- The trend continues for DDI migrating to TDDI and OLED. Our 12-inch royalty will benefit from increasing TDDI and OLED applications.
- There are more tape-outs at 28nm for STB, Multimedia and Network-related applications. These products will contribute to our royalty in 2018 and beyond.
- Our NeoFuse solution will be adopted in 25nm DRAM for memory repair function and will contribute to royalty growth in the future.

Outlook for Q4 and beyond

- **R&D developments**

- › **Our NeoFuse IP has been verified successfully at 7nm process in the major foundry.**
- › **We continue to develop 7/12/14nm and 22nm SOI with major foundries.**
- › **We have started emerging memory development with a major US IDM.**
- › **Our security IP NeoPUF has been proven at a major foundry and has the first customer tape-out product this year.**

Key Growth Drivers

Growth in application per mobile devices

- More chip applications per smartphone/tablet product.

Growth into more markets

- From consumer electronics and mobile devices to wearable devices.
- Adding new NVM product lines further enable more product applications.

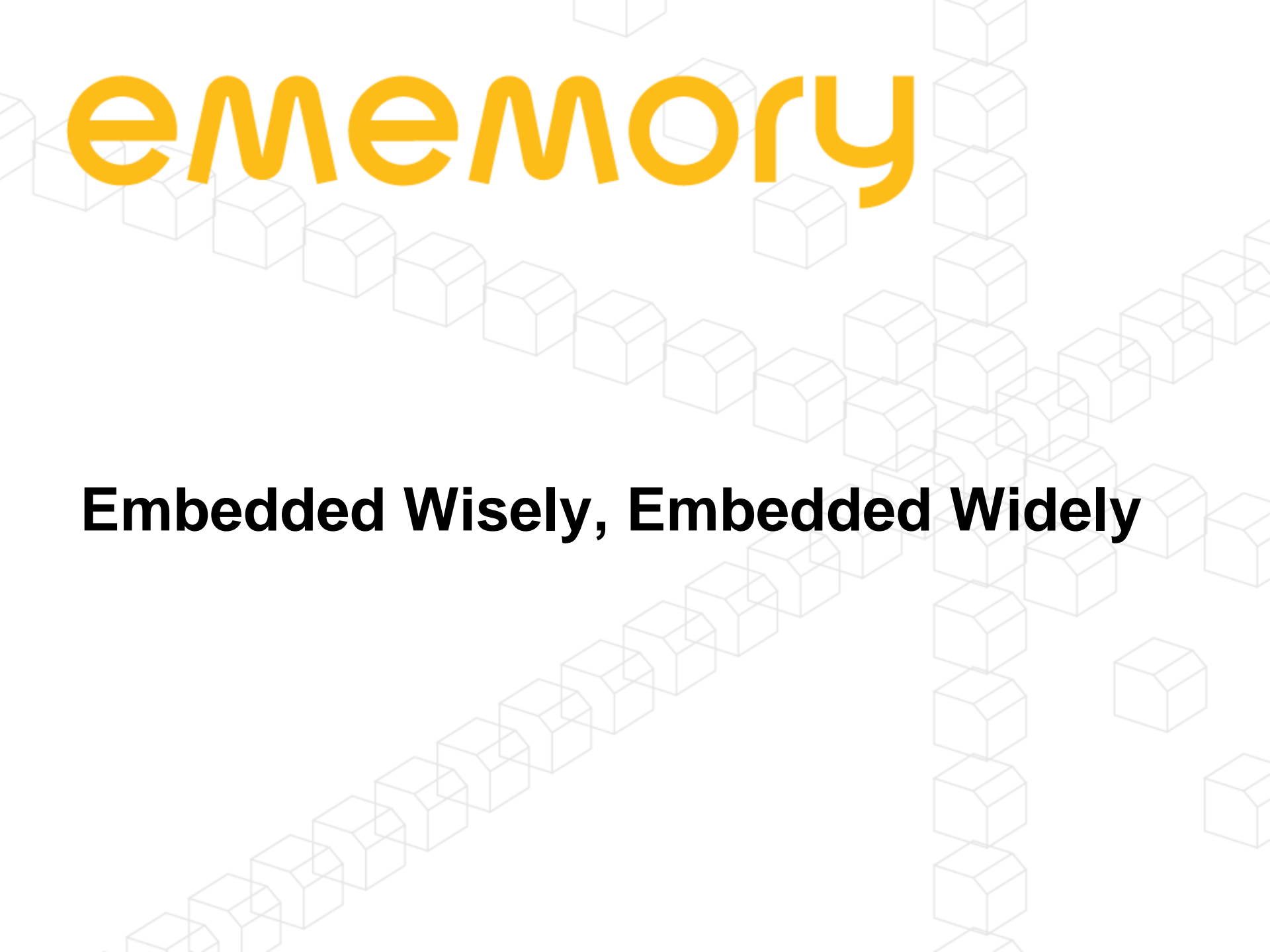
Growth in advanced technology

- Higher royalty per wafer is contributed from more advanced technology nodes.

Great IoT era

- Embedded Logic NVM will be a must.

Q & A



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Embedded Wisely, Embedded Widely