ememory

力旺電子(3529)

A Leading Logic NVM Company

智慧財產權聲明

本文件內之資訊，包括文字、圖片、圖表、表格或其他檔案等，其所有權利或利益，包括但不限於所有權及智慧財產權，皆屬力旺電子所有，請尊重智慧財產權。本文件之內容包含力旺電子之機密資訊。部分內容可參見2014年出版之Logic Non-Volatile Memory (The NVM solutions from eMemory)一書。任何在此之資訊在未經力旺電子書面同意，不得影印、散佈、複製、使用本文件或將其揭露予第三人。

eMemory, NeoBit, NeoFuse, NeoFlash, NeoEE, NeoMTP, NeoROM, EcoBit與NeoPUF皆為力旺電子在台灣或其他國家之商標或服務標章。

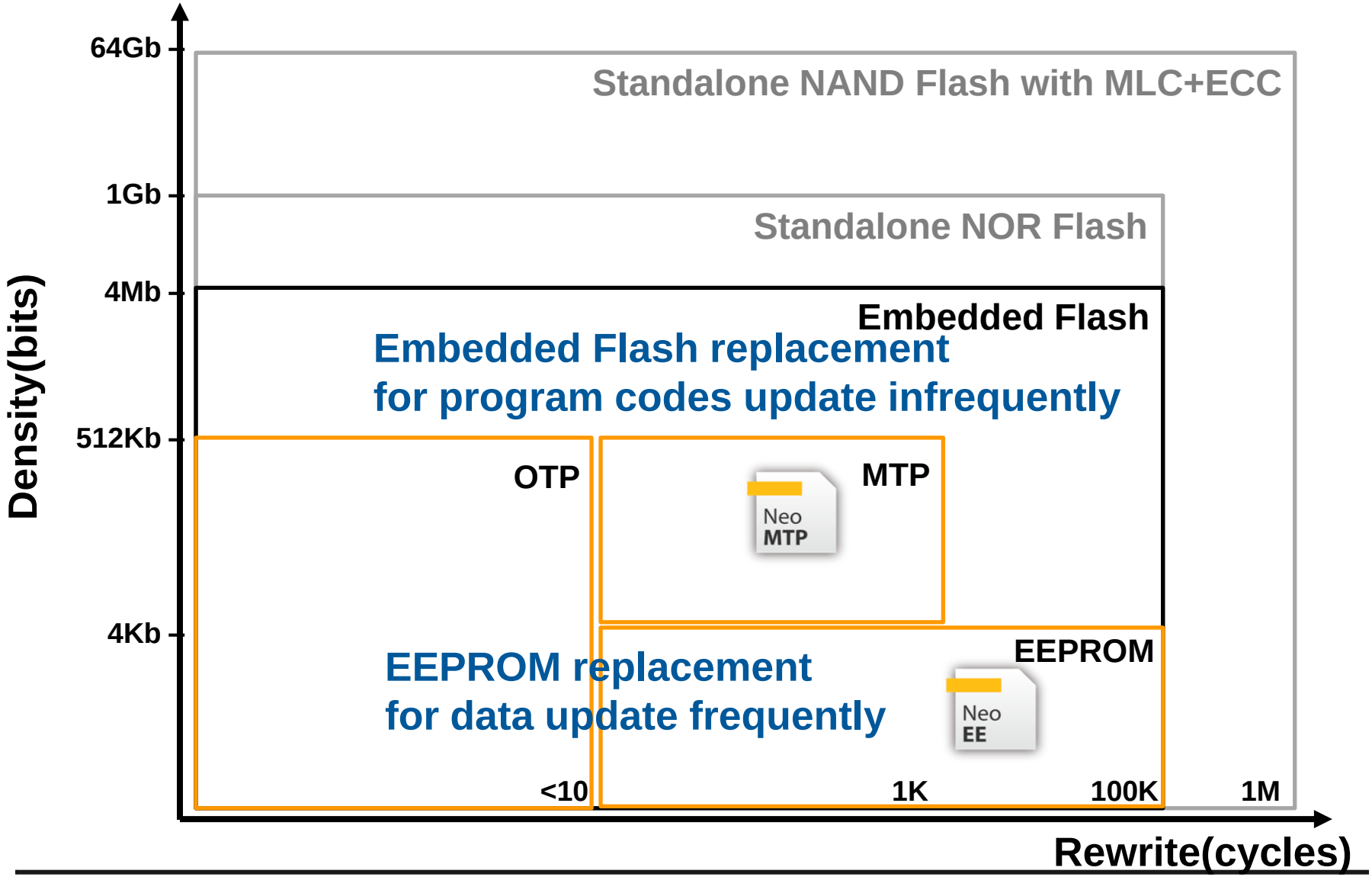
投資安全聲明

除簡報內所提供之歷史信息外，簡報事項係屬預測性陳述，受到風險及不確定性因素影響，可能造成實際結果與陳述內容發生不符，這些不確定性因素包括：技術平台是否順利導入利用、IP是否被客戶接受、客戶產品大量量產之能力及時間、產業及市場對半導體產品之供給及需求移轉、終端市場之穩定性及其他風險等。

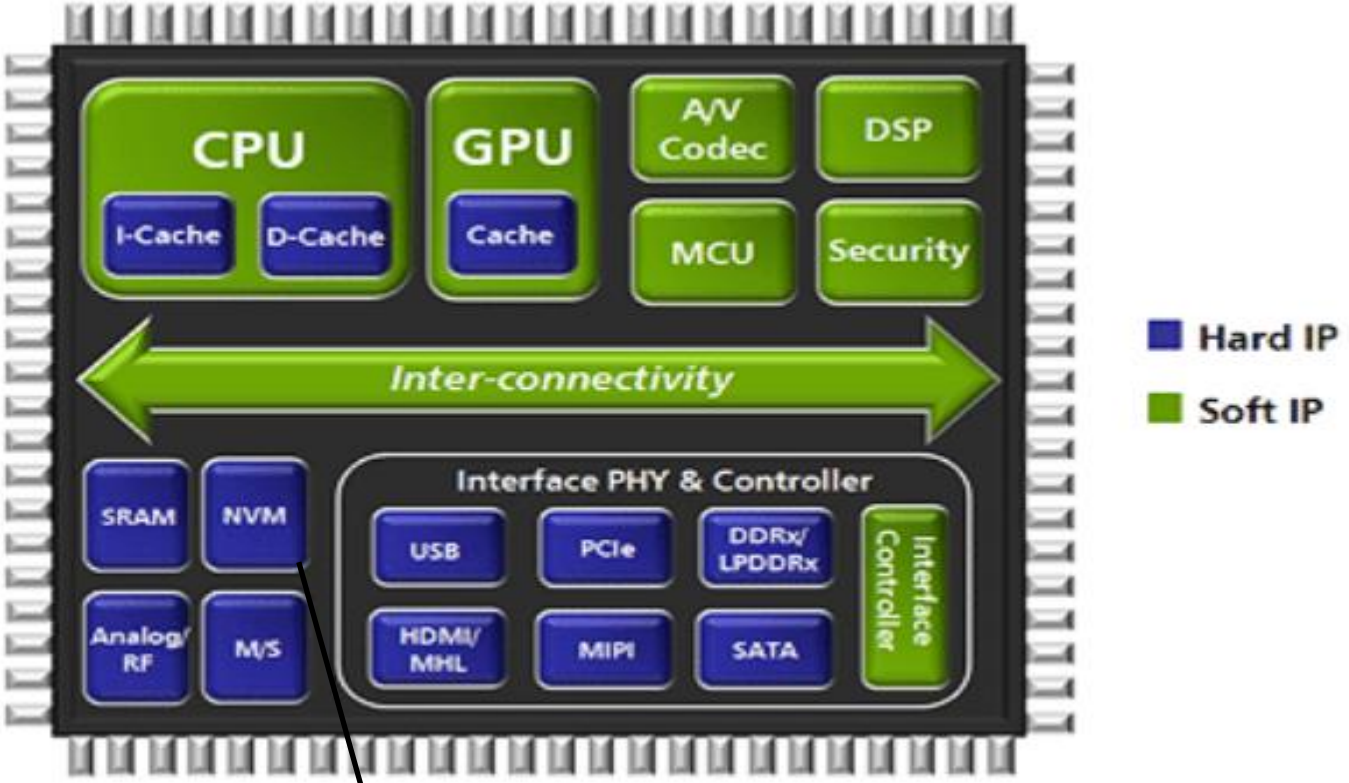
大綱

- 公司營運模式
- 營運回顧
- 成長機會與未來展望
- 問題與回答

嵌入式非揮發性記憶體分類



SOC Block Diagram



Embedded Non Volatile Memory

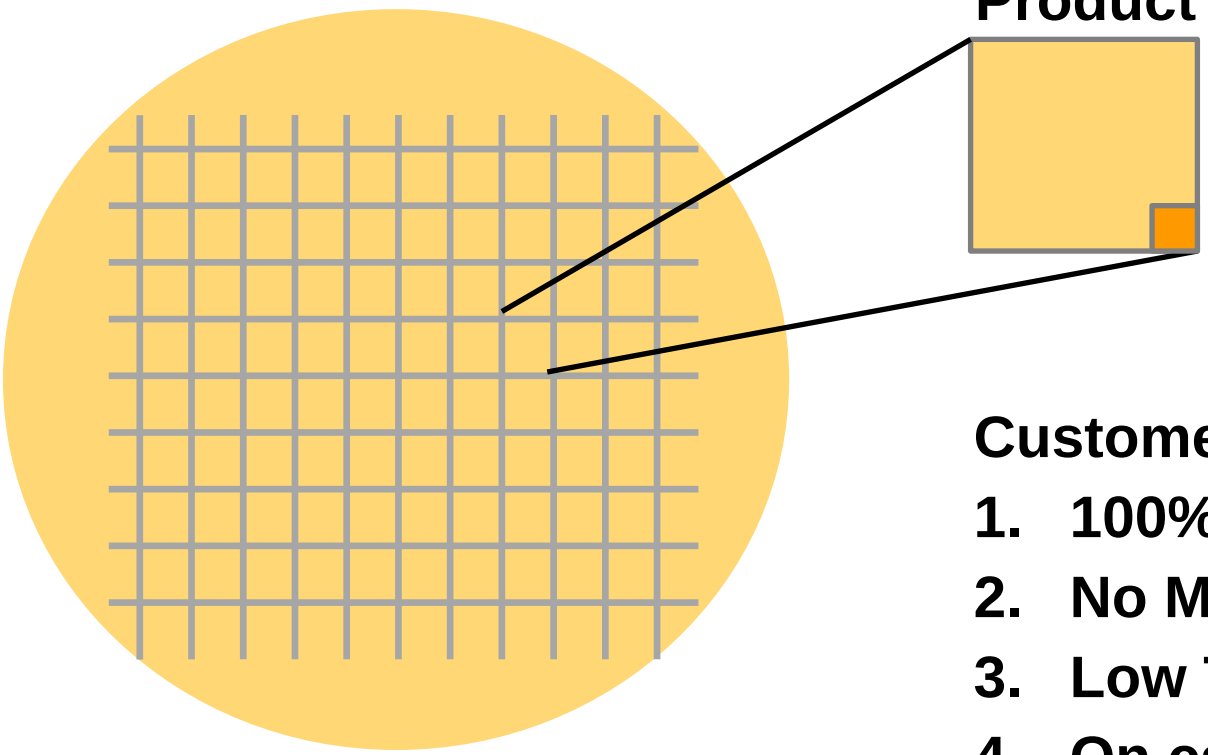
Source : tsmc

嵌入式非揮發性記憶體技術

	ROM	eFuse (OTP)	Antifuse (OTP)	CMOS Floating Gate (OTP)	CMOS Floating Gate (MTP)	Embedded Flash
Cell Structure	Transistor	Poly Fuse	Antifuse	Floating Gate	Floating Gate	Floating Gate
Standard CMOS Compatible	Yes	Yes	Yes	Yes	Yes	No
Bitcell Area	< 1	50	1	2	4	1
Endurance	No	No	< 10	< 10	10K-100K	100-1000K
Density	4Kb-1Mb	256bit-4Kb	16bit-1Mb	16Kb-1Mb	1Kb-2M	64Kb-4Mb
Security	Low	Low	High	High	High	High
Additional Steps	None	None	None	None	None	+10 Mask

- ROM not programmable, eFuse cannot scale beyond 16Kb, embedded flash expensive and cannot scale after 40 nm
- eMemory's IPs: OTP (antifuse, floating gate) and MTP (floating gate)

採用IP之考量

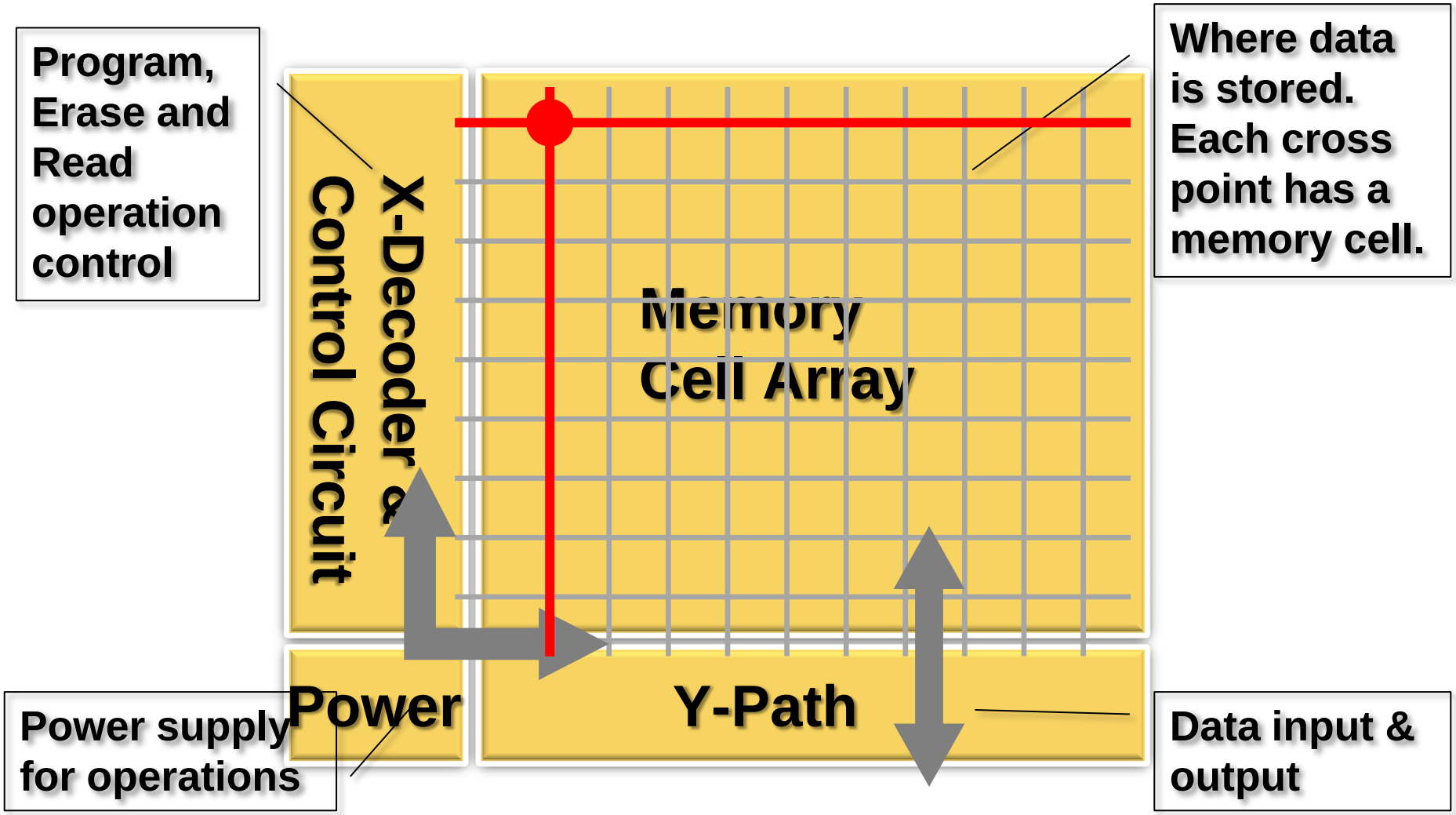


Generally,
IP size is less than
10% of product size

Customers Request

1. **100% IP Reliability**
2. **No Mask Adder**
3. **Low Testing Cost**
4. **On call Service**
5. **Acceptable IP Size**

Nonvolatile Memory IP 內部



關於力旺

2000年成立 → 2002年第一個客戶 → 2005年開始獲利 → 2011年掛牌上市

- 全世界最大的邏輯非揮發性記憶體IP公司
- 238位員工，其中166位為研發人員*
- 2011年掛牌以來，無市場籌資，無銀行借款
- 每年的現金配息率超過90%

註*: 截至 2017/09/30

營運模式

- 成長性指標:
  - 正在晶圓廠建構的製程平台數
  - 設計授權數
  - 權利金

前期授權金
=技術授權金 + 設計授權金

1-2 years
eMemory & foundry development

Technology License Revenue

1-2 years
Fabless product development

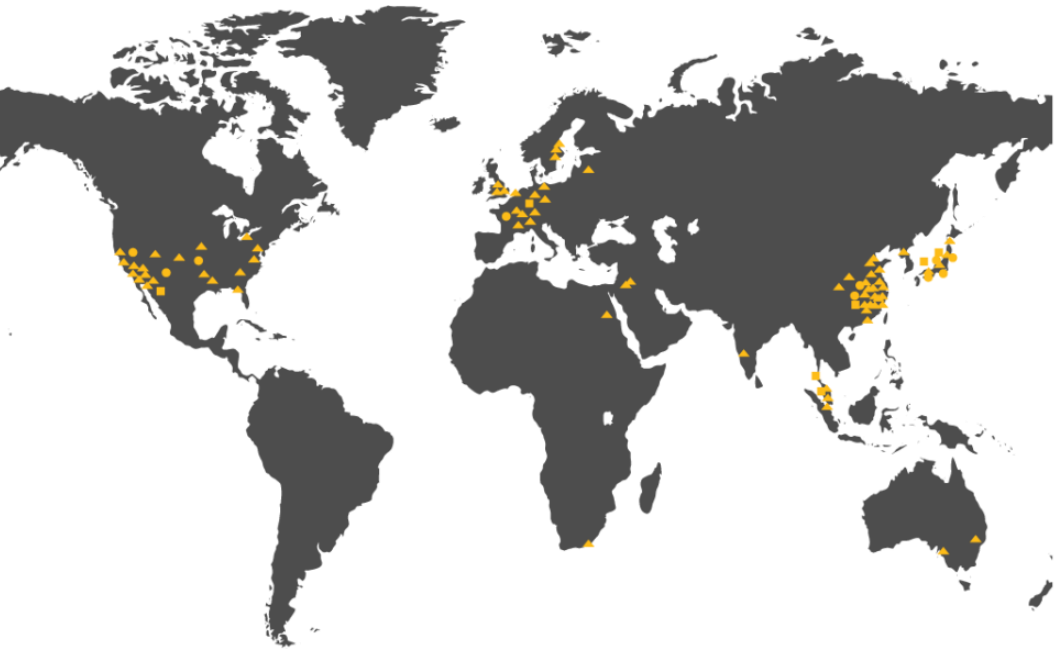
Design License Revenue

3+ years
Multiple application & sales

Royalty Revenue Continues

權利金
=客戶於晶圓量產時向晶圓廠收取

全球客戶



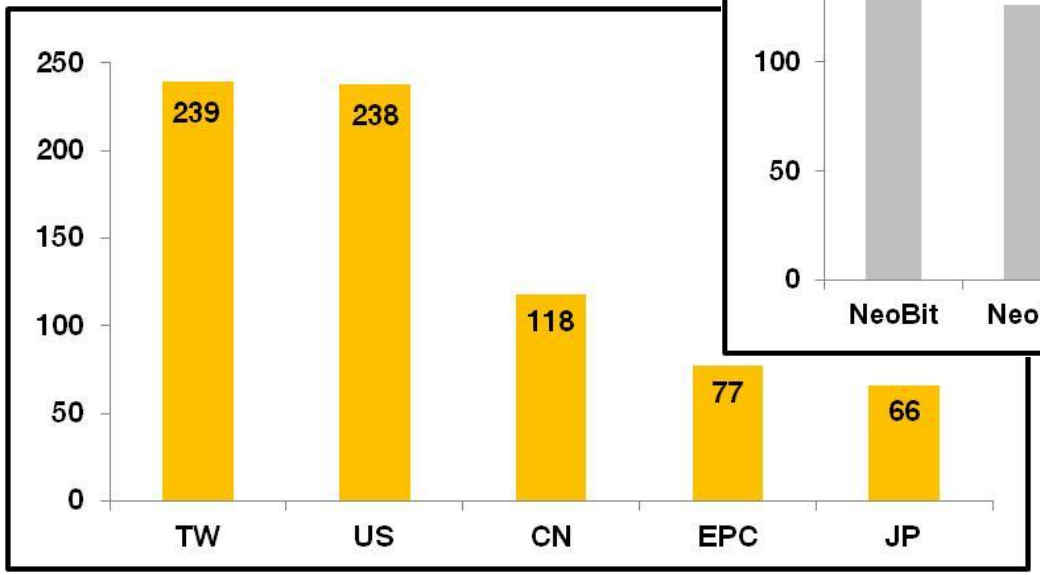
	Taiwan	China	Korea	Japan	North America	Europe	Others
Foundry	5	8	3	4	1	2	1
IDM	0	0	0	8	2	1	0
Fabless	261	513	71	52	242	111	53

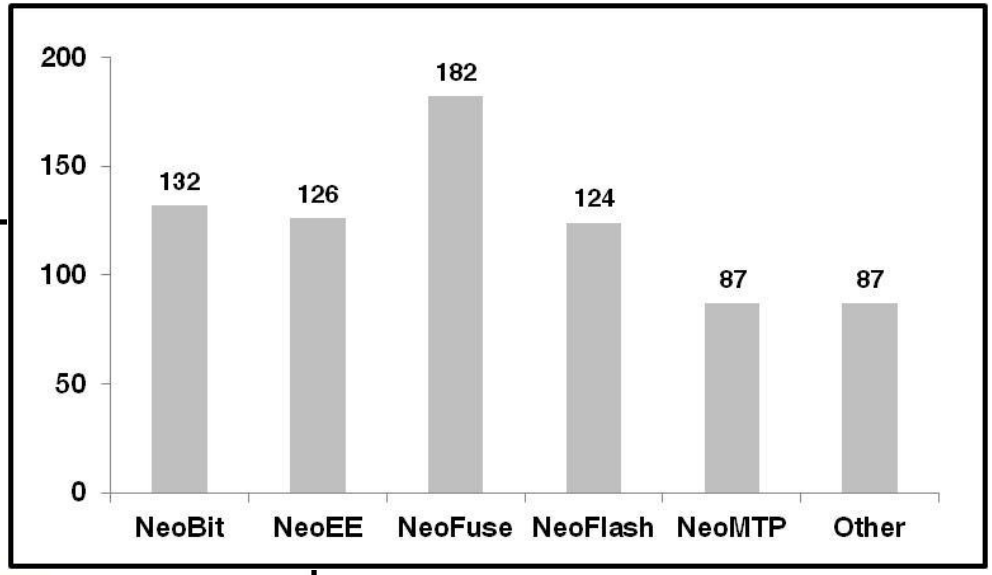
Foundry

IDM

專利佈局

	2Q 17	3Q 17	Change
Pending	232	252	+ 20
Issued	453	486	+ 33
Total	685	738	+ 53



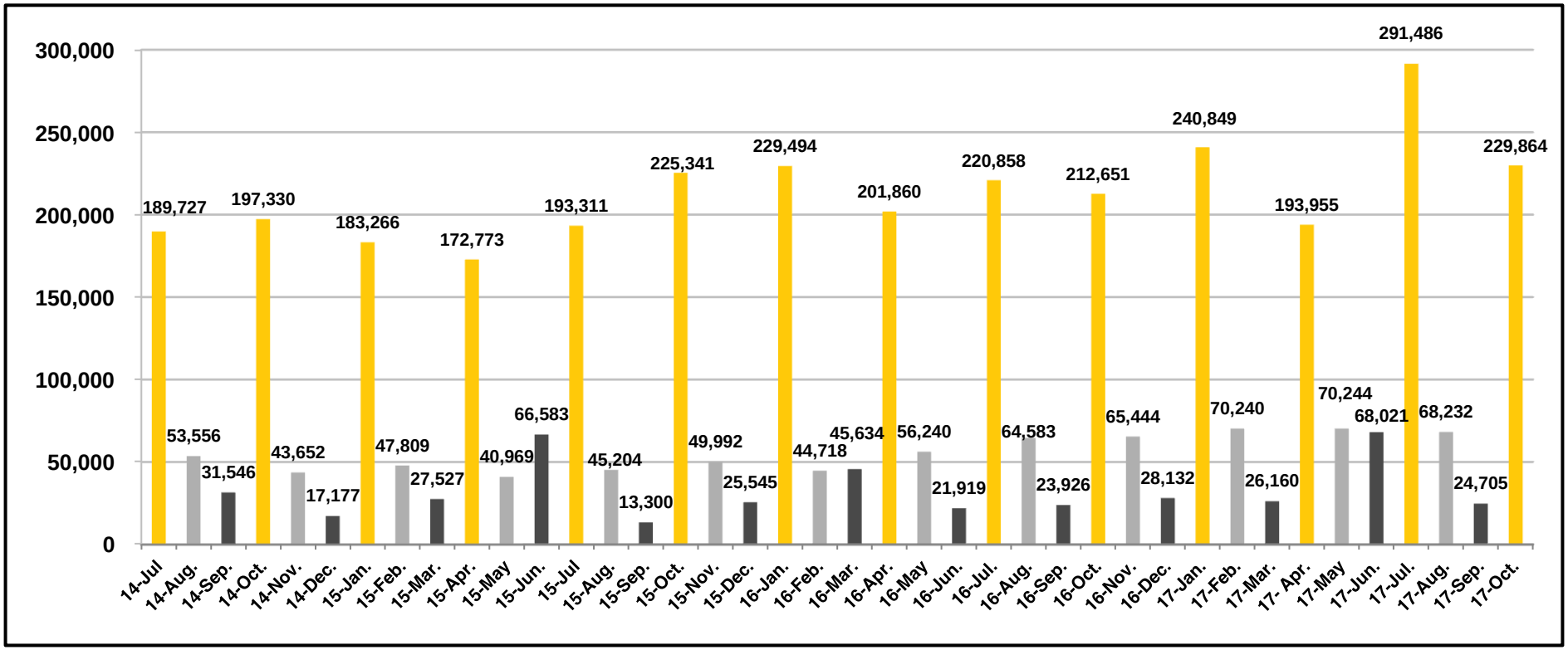


Note: As of Sep. 30th, 2017

每季營收模式

- 每季第一個月認列絕大部份晶圓廠前一季使用本公司IP的出貨晶圓權利金及當月產生的技術授權金及設計授權金；第二個月則是少部份晶圓廠權利金及當月授權金；第三個月則無權利金收入，只有授權金。

單位：台幣仟元



大綱

- 公司營運模式
- 營運回顧
- 成長機會與未來展望
- 問題與回答

第三季各項營收

單位：新台幣仟元

K NTD	Q3 2017	Q2 2017	QoQ	Q3 2016	YoY	Q1 – Q3 2017	Q1 – Q3 2016	YoY
授權費	101,087	134,140	-24.6%	86,712	16.6%	309,373	250,403	23.6%
權利金	283,336	198,080	43.0%	222,655	27.3%	744,519	658,829	13.0%
合計	384,423	332,220	15.7%	309,367	24.3%	1,053,892	909,232	15.9%

單位：合約數

		Q3 2017	Q2 2017	2016	2015
技術授權數		4	8	43	28
設計授權數	NRE	23	13	56	57
	使用費	87	77	311	349

綜合損益表

(單位:新台幣仟元)	Q3 2017	Q2 2017	Q3 2016	change (QoQ)	change (YoY)
營業收入淨額	384,423	332,220	309,367	15.7%	24.3%
營業毛利率	100%	100%	100%	-	-
營業費用	205,291	188,562	173,605	8.9%	18.3%
營業淨利率	46.6%	43.2%	43.9%	3.4ppts	2.7ppts
本期淨利	194,062	135,610	130,299	43.1%	48.9%
純益率	50.5%	40.8%	42.1%	9.7ppts	8.4ppts
每股盈餘 (單位: 新台幣元)	2.56	1.79	1.72	43.0%	48.8%
權益報酬率	40.2%	29.6%	28.9%	10.6ppts	11.3ppts

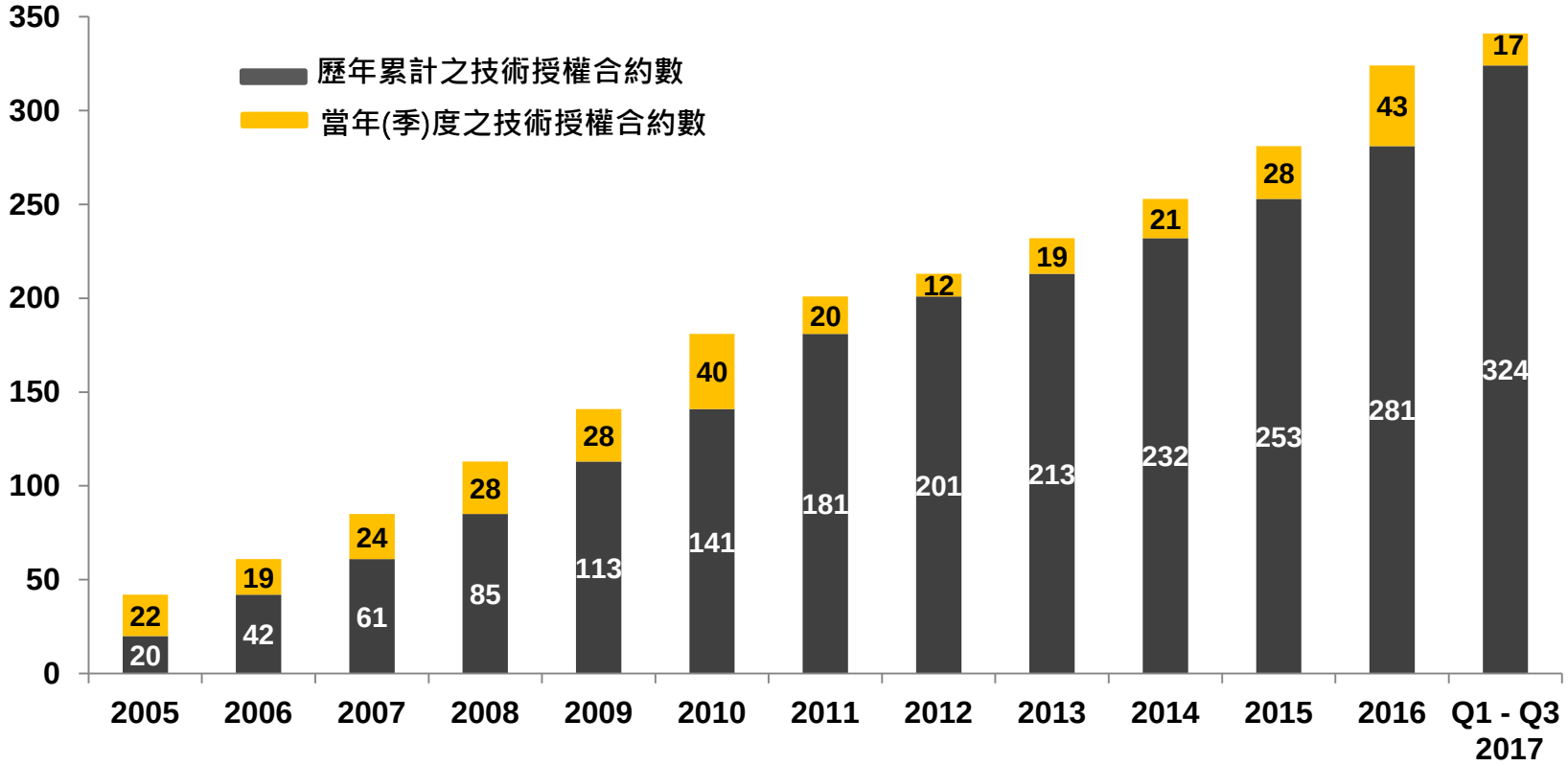
Note：美金營收, QoQ 成長15.5%，YoY成長30.4%。

技術授權合約

單位：合約數

Year	2014	2015	2016	Q1- Q3 2017
License	21	28	43	17

註: 與晶圓廠簽訂的技術授權合約所含的技術製程及授權金視合約內容而定，無特別季節性因素。



目前正在建構的技術製程平台

- New technologies being developed for 108 platforms by Q3 17.
- 21 for NeoBit, 42 for NeoFuse, 19 for NeoEE, and 26 for NeoMTP.

	7/10nm	12/14/16nm	28nm	40nm	55/65nm	80/90nm	0.11~ 0.13um	0.15~ 0.18um	>0.25 um
NeoBit	-	-	-	-	-	-	9	12	-
NeoFuse	3	3	7	5	10	7	3	4	-
NeoEE	-	-	-	-	-	-	2	17	-
NeoMTP	-	-	-	1	1	2	7	15	-

註: 截至 2017/09/30

目前正在建構的技術製程平台

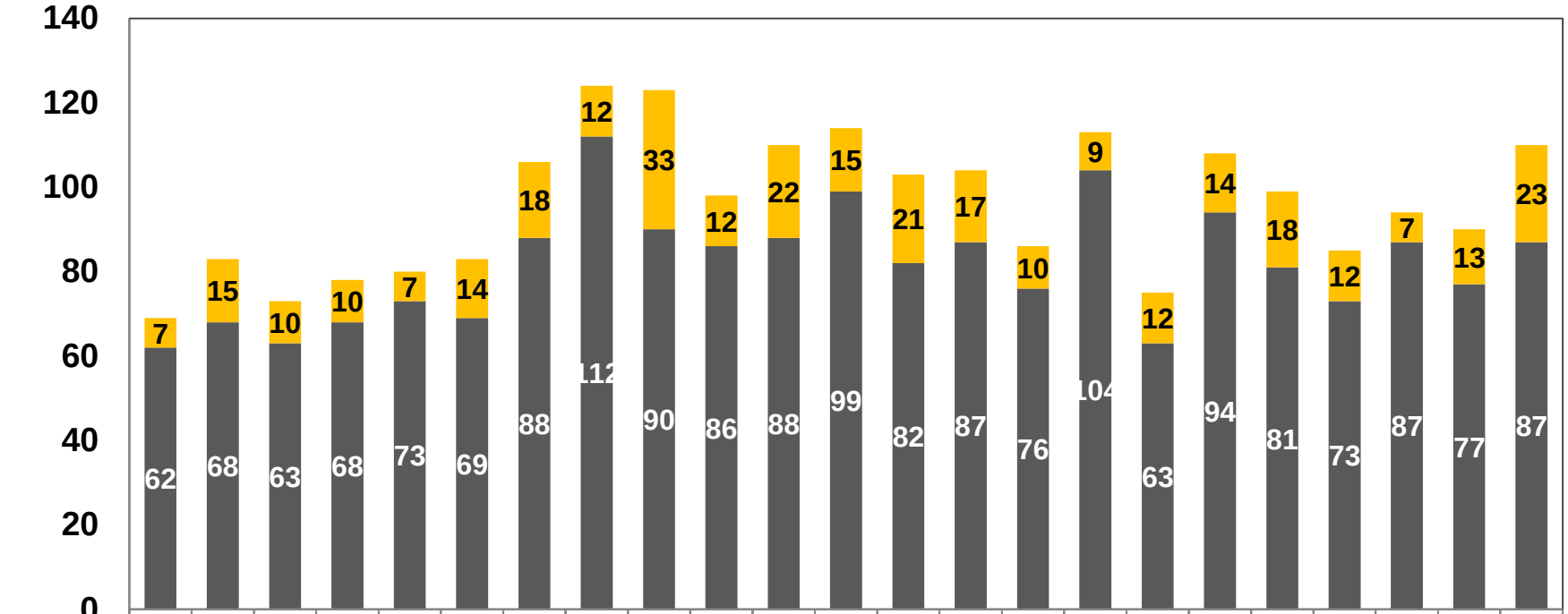
12" Fabs	Production	Development	NVM Type	Process Type
7/10nm	0	3	OTP	FF
12/14/16nm	2	3	OTP	FF+
28nm	9	7	OTP	LP/HPM, HLP/HPM, LPS
40nm	8	6	OTP, MTP	HV-DDI, LP, eFlash
55/65nm	14	11	OTP, MTP	LP, HV-DDI, HV-OLED, DRAM, CIS, eFlash
80/90nm	6	6	OTP, MTP	HV-DDI, HV-OLED, LP, eFlash
0.13/0.11um	9	1	OTP	HV-DDI, BCD, Generic
0.18um	1	0	OTP	BCD
Total	49	37		

8" Fabs	Development	NVM Type	Process Type
90nm	3	OTP	HV-DDI, LL
0.13/0.11um	20	OTP, MTP	HV-DDI, BCD, LP, RF, CIS, LL, Green
0.18/0.16/0.152um	48	OTP, MTP	Generic, LP, LL, MR, HV, Green, BCD
0.25um	0	OTP, MTP	BCD
0.35um	0	OTP	UHV
Total	71		

註: 截至 2017/09/30

每季設計授權數(New Tape-Out)

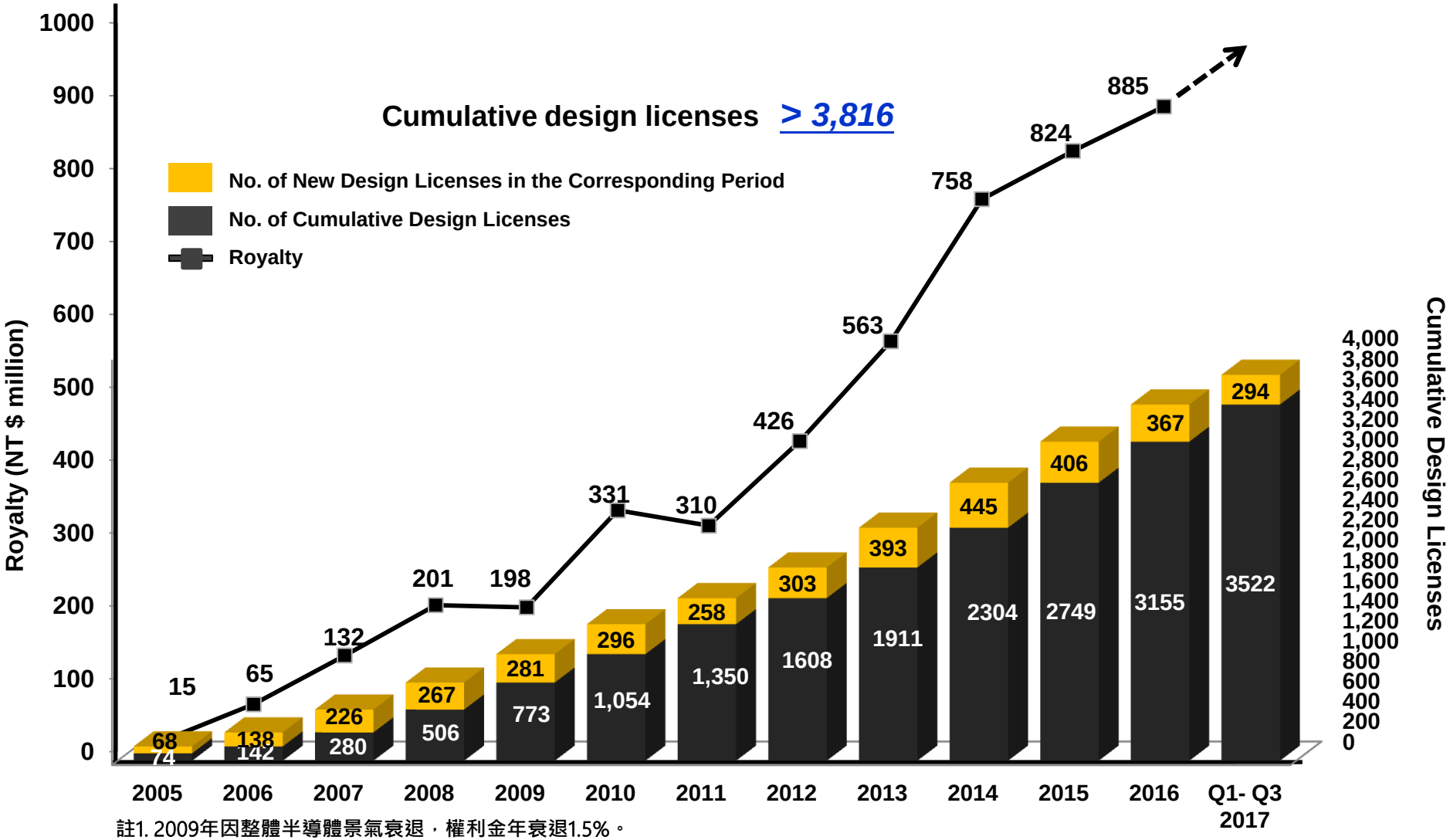
- A total 294* NTO in Q1-Q3 2017 *(367@2016, 406@2015, 445@2014, 393@2013)



	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3
	2012				2013				2014				2015				2016				2017		
NRE	7	15	10	10	7	14	18	12	33	12	22	15	21	17	10	9	12	14	18	12	7	13	23
Usage	62	68	63	68	73	69	88	112	90	86	88	99	82	87	76	104	63	94	81	73	87	77	87

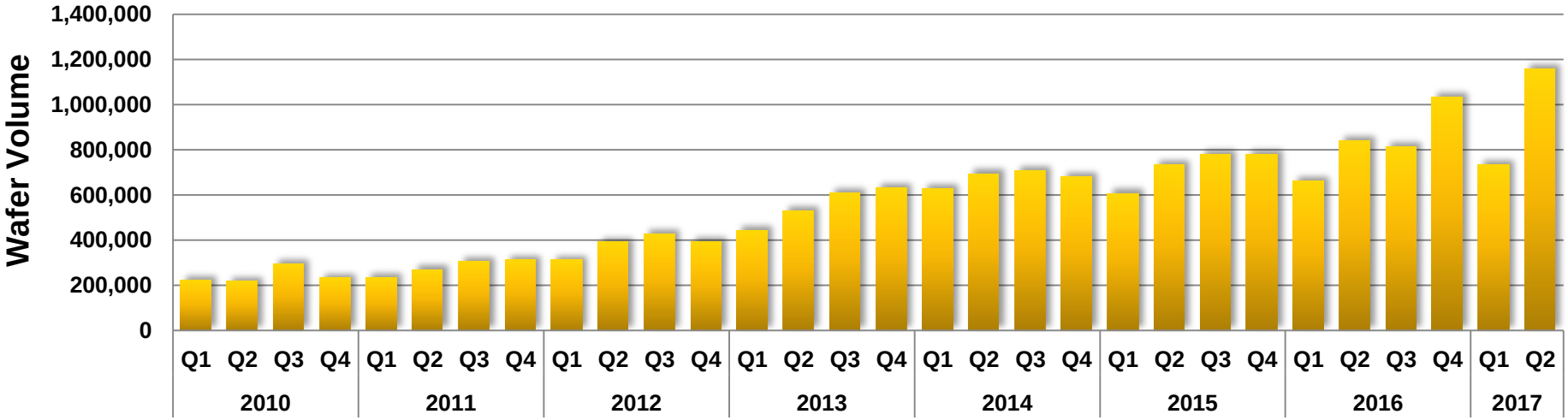
註：客戶在各代工廠的諸多MCU NTO已陸續進入量產，加上與主要Green process代工廠的商業模式商業模式調整為直接license IP cell 給代工廠，由代工廠提供設計服務給客戶，造成tape out 數減少，但仍對使用IP cell 的晶片支付權利金. 雖然MCU的NTO數量有明顯減少，但是相關的晶圓產出和權利金收入還是持續增加

權利金取決於過去累積的設計授權數



註1. 2009年因整體半導體景氣衰退，權利金年衰退1.5%。
註2. 2011年因2010年單一客戶預付權利金，導致2010年成長67%，2011年年衰退6.3%。
註3. 2009-2013年權利金年複合成長率為30%。

每季量產晶圓片數



eMemory IP's Penetration Rates in T Company (in US $ revenue)

	Process node	*% of T	Q3 17	Q2 17	2016	2015
8"	0.25/0.35	2%	34.06%	44.84%	28.15%	33.49%
	0.15/0.16/0.18	10%	7.93%	7.36%	12.43%	8.73%
	0.11/0.13	3%	55.97%	58.76%	42.61%	29%
12"	80/90nm	5%	13.88%	12.73%	12.50%	19.85%
	55/65nm	10%	2.22%	4.73%	3.59%	0.55%
	40/45nm	12%	0.12%	0%	0%	0%
	28nm	23%	0.01%	0.18%	0.55%	0.05%
	16/20nm	24%	0%	0%	0%	0%
	10nm	10%	0%	0%	-	-
8"		16%	20.34%	21.77%	18.86%	16.64%
12"		84%	1.13%	1.43%	1.44%	1.87%
Total		100%	4.20%	5.07%	4.27%	4.76%

* T company's Q3 2017 revenues broken down by process nodes, the royalty was recognized in eMemory's Oct. revenue.

大綱

- 公司營運模式
- 營運回顧
- 成長機會與未來展望
- 問題與回答

力旺之NVM技術

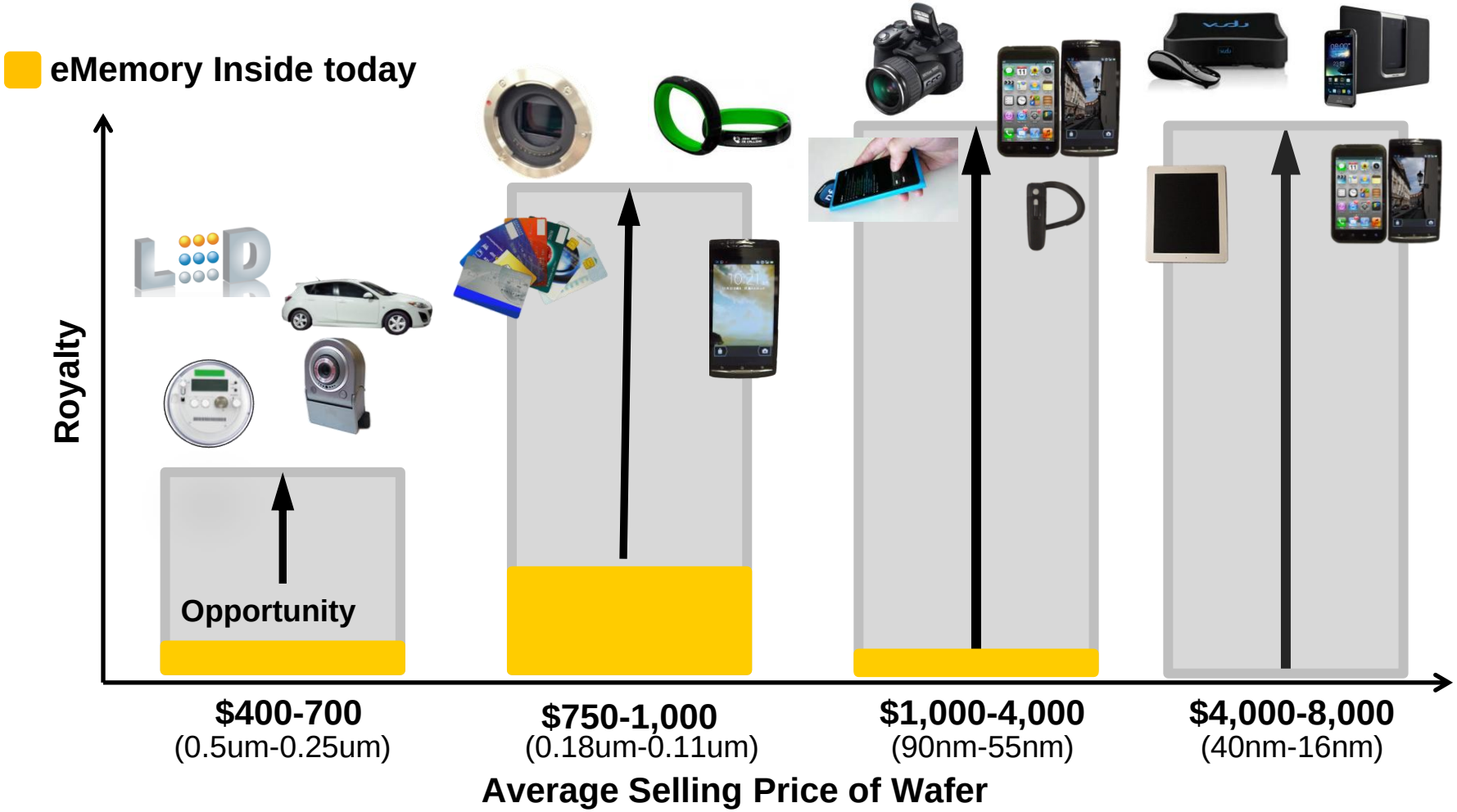
- **Logic NVM portfolio offers one-stop-shop solution.**
  - Compatible to any process
  - Robust structure
  - Low process cost
  - Competitive macro sizes
  - Easy integration
  - Easy porting

eMemory's NVM Technology	OTP		MTP		
	NeoBit	NeoFuse	NeoFlash	NeoEE	NeoMTP
Product Type	OTP	OTP	Flash	EEPROM	MTP
Endurance (Cycles)	10	10	1K~10K	10K~100K	1K~10K
Additional Mask Steps	0	0	2-3	0	0
Technology	Floating gate	Anti-Fuse	SONOS	Floating gate	Floating gate
Scalability	Simple	Simple	Simple	Simple	Simple
Memory Density	HD < 512Kb GHD < 16Mb	< 4Mb	< 2Mb	< 4Kb	< 512Kb

力旺IP的應用

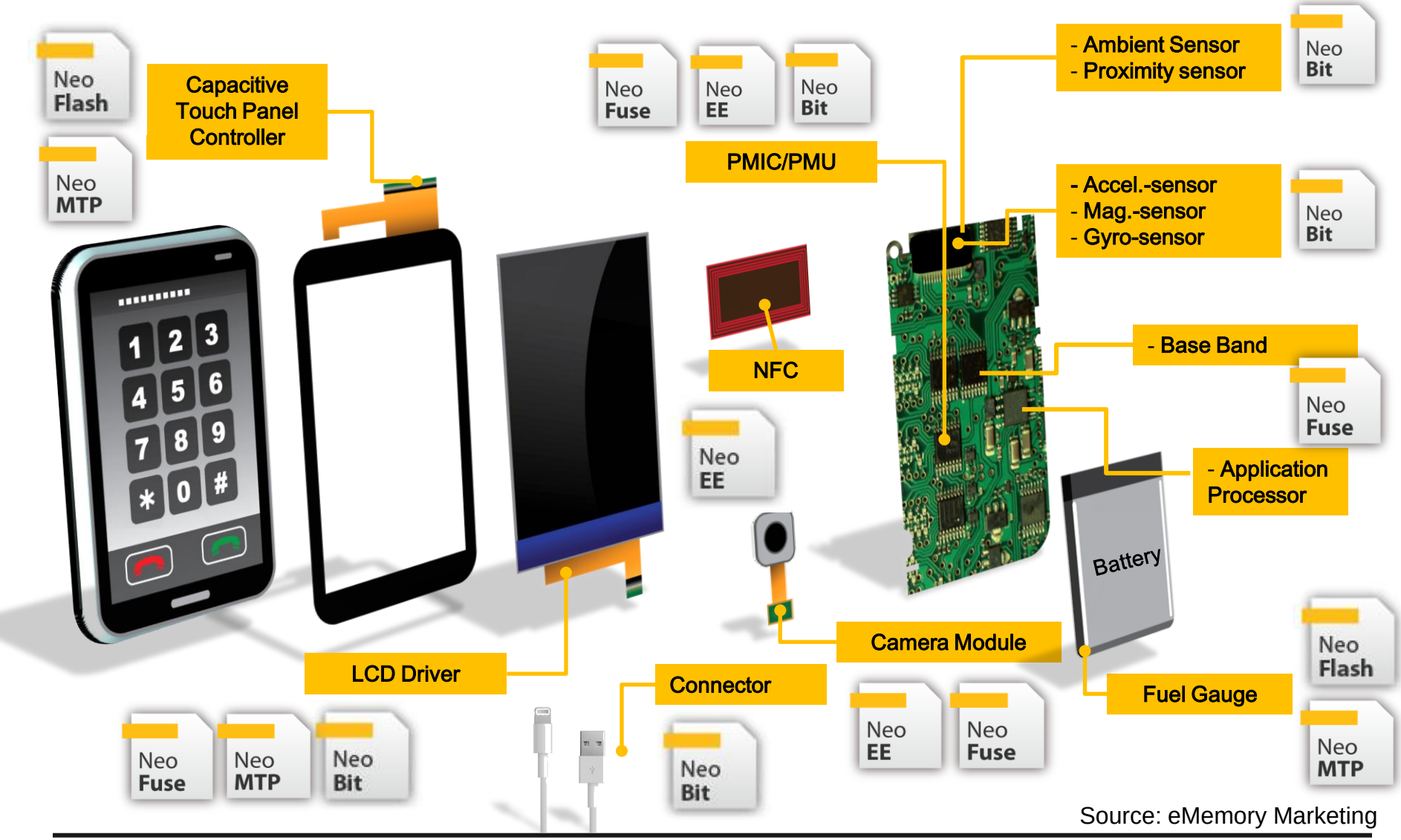
12"								8"		
7nm	10nm	12/14/16nm	28nm	40nm	55/65nm	80/90nm	110/130nm	160/180nm	250nm	350nm

商機與潛力



Note: 2.2 million 8” equivalent wafers with eMemory IP were shipped in 2013. (~5% of WW foundry shipment)

智慧型手機中力旺 IP 的應用

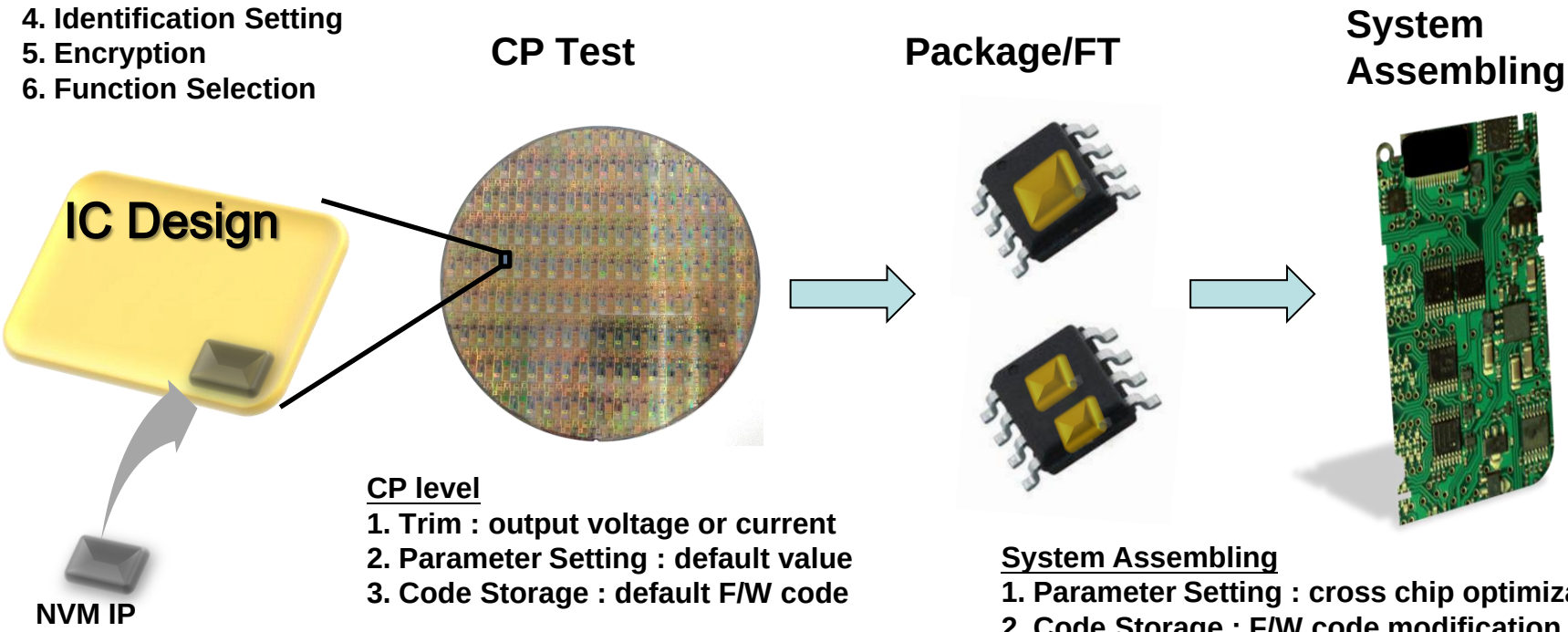


Source: eMemory Marketing

Benefits from Using eMemory IPs

Design-in for
1. Trimming
2. Parameter Setting
3. Code Storage
4. Identification Setting
5. Encryption
6. Function Selection

Package/FT level
1. Trim : SPEC shift
2. Parameter Setting : cross chip optimization
3. Identification Setting : manufacturer resume
4. Function Selection : setting for target market



CP level
1. Trim : output voltage or current
2. Parameter Setting : default value
3. Code Storage : default F/W code

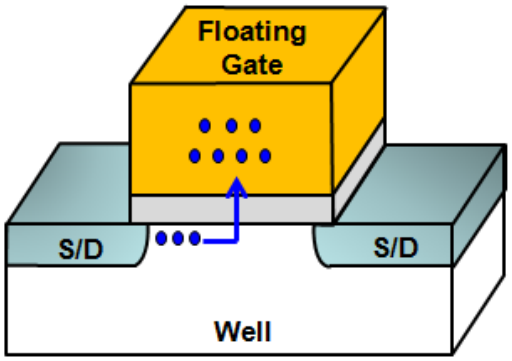
System Assembling
1. Parameter Setting : cross chip optimization
2. Code Storage : F/W code modification
3. Identification Setting : manufacturer resume
4. Encryption : Security algorithm or key storage

高機密性的安全設定

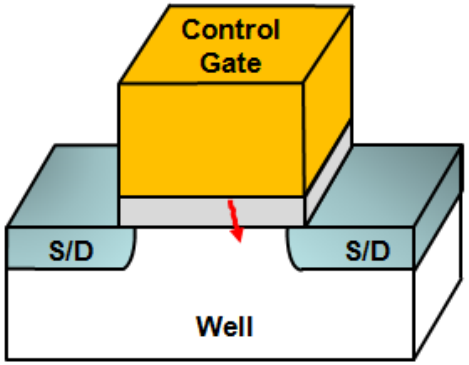
- Provide “Invisible Hardware Key” for invisible storage
- Prevent reverse-engineering to detect content of security key
- Protect firmware and hardware of ICs from pirating
- Extend & protect customer’s business

eFuse Key: Data is easily observed

Invisible Hardware Key : Data is hard to be detected



Floating Gate



Anti-Fuse

硬體設計防護

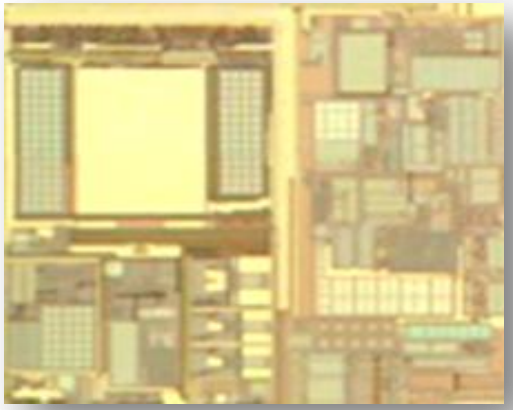
Authorized Product

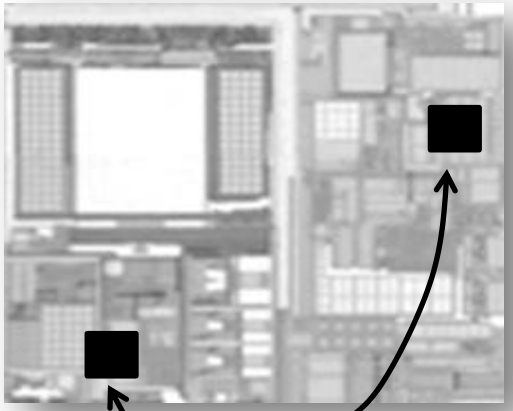
Fake Product

reverse copy

re-produce

without protection

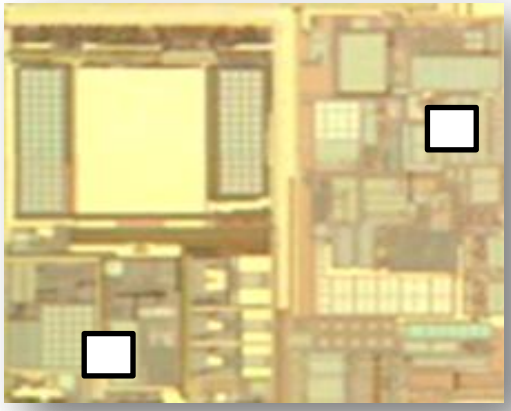




reverse copy

re-produce

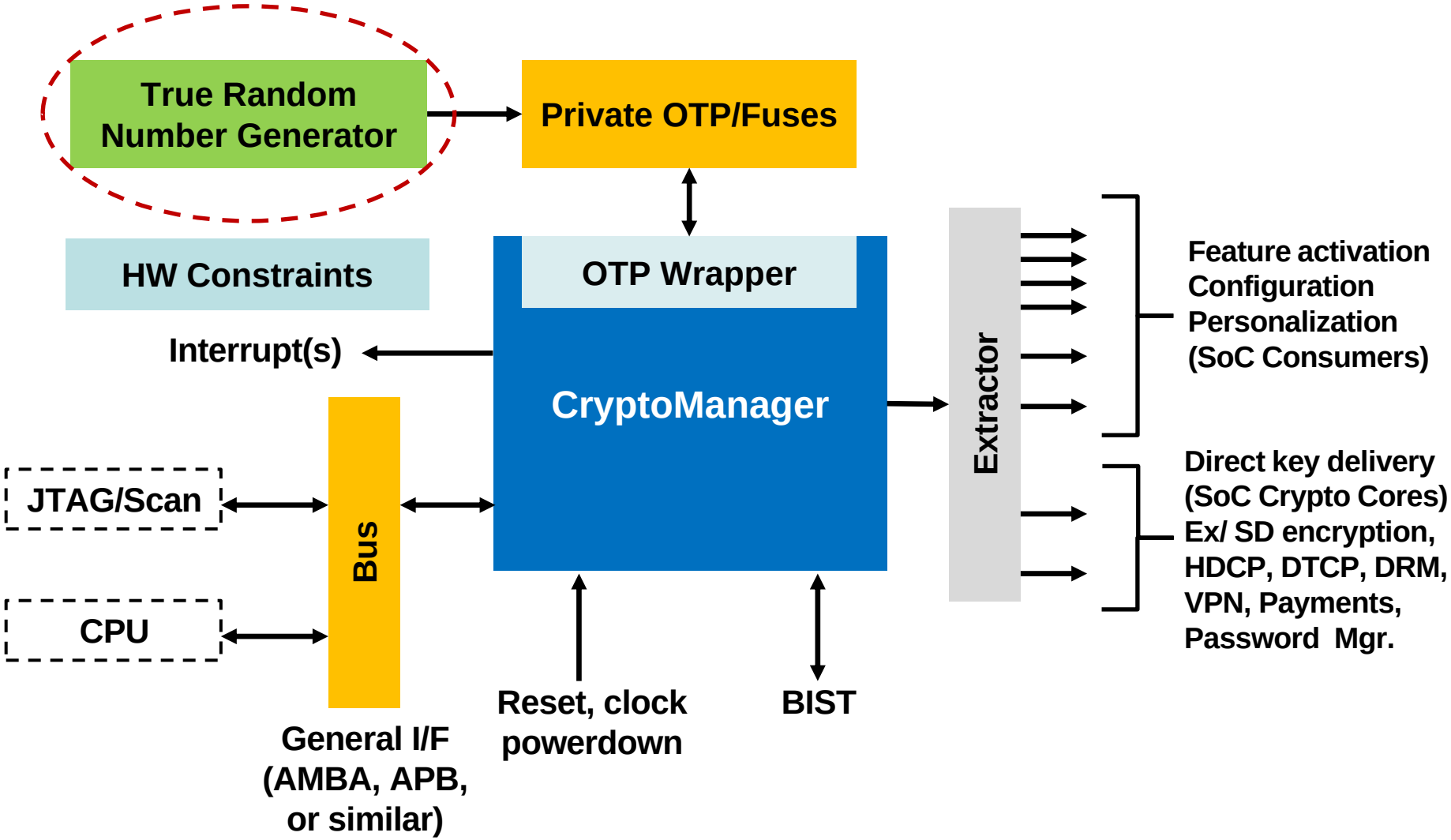
with protection



Security IP/Code by Authorized Use

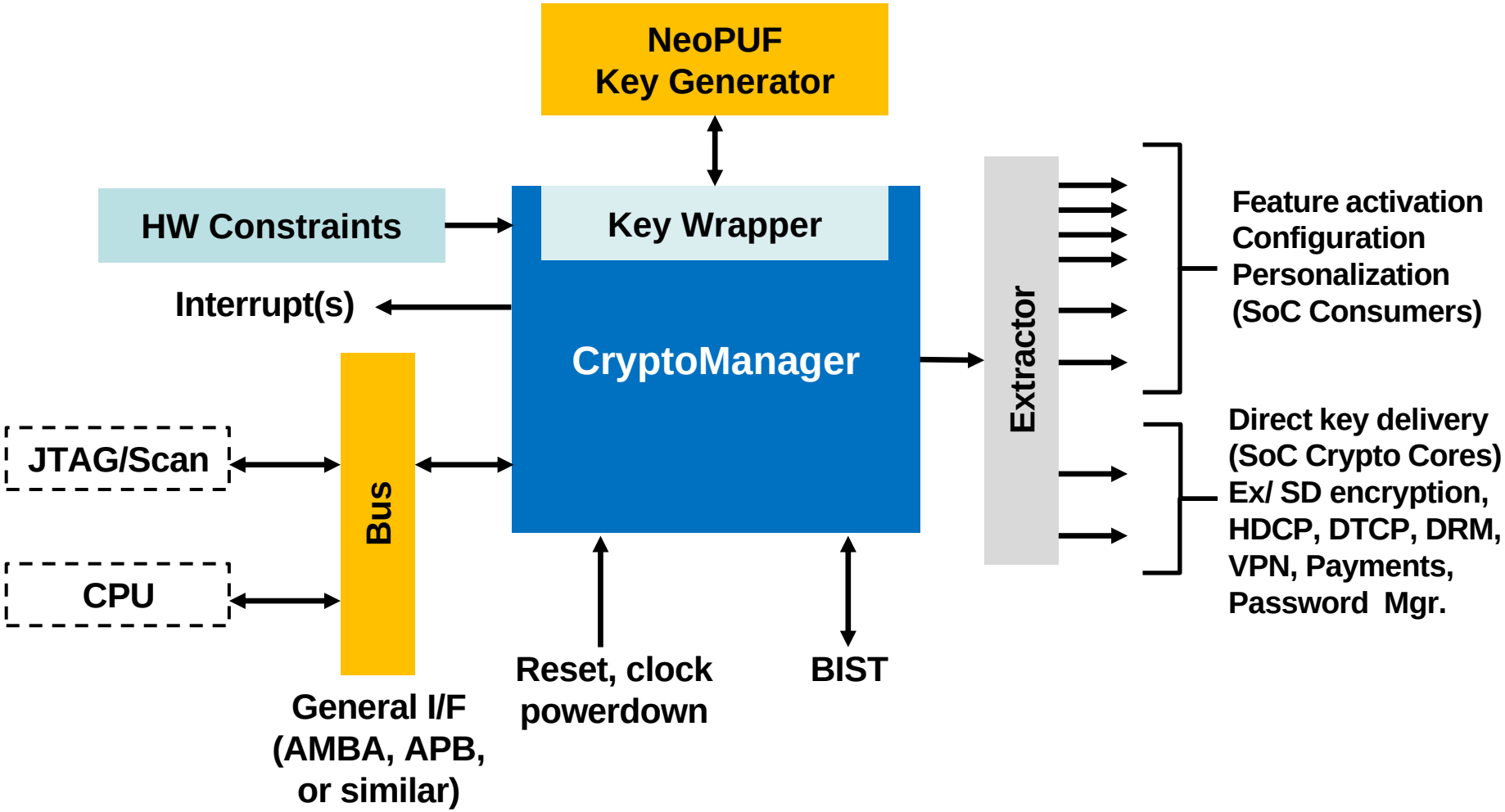
Can NOT Work w/o Security IP/Code

OTP在加密儲存應用



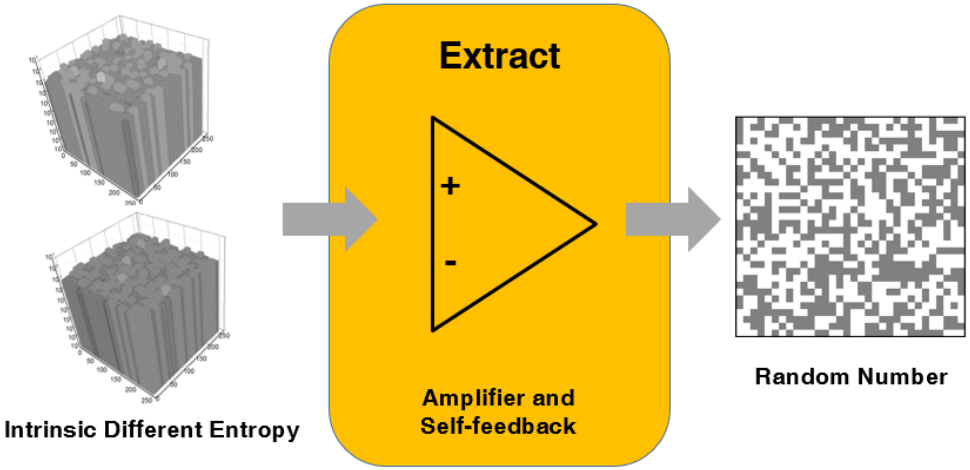
Source： Rambus crypto manager platform

NeoPUF在加密金鑰的應用



Source： Rambus crypto manager platform

何為 PUF (Physical Unclonable Functions)

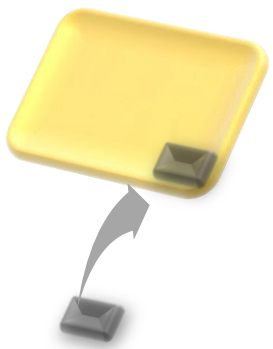


Collision Probability ≒ 1/15B ≒ $1/2^{34}$

Collision Probability = $1/2^{\text{Bits Stream Length}}$

NeoPUF技術

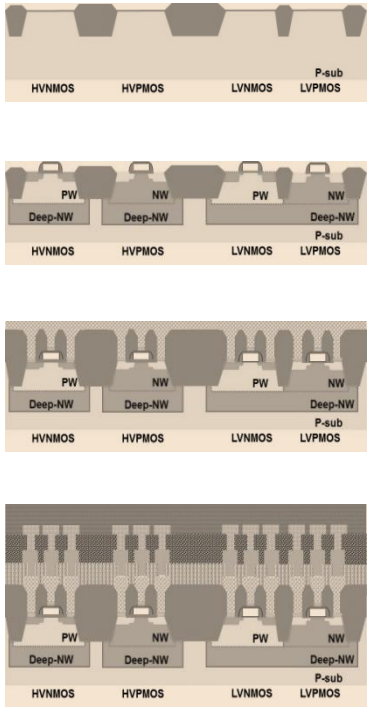
IC Design



eMemory IP

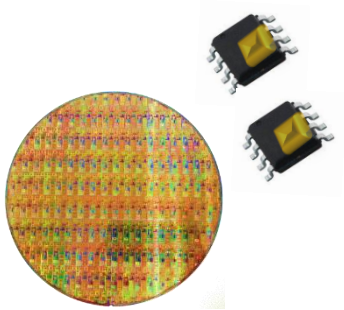
Design-in
Customized SPEC & Function are designed for customer demands

Wafer Process



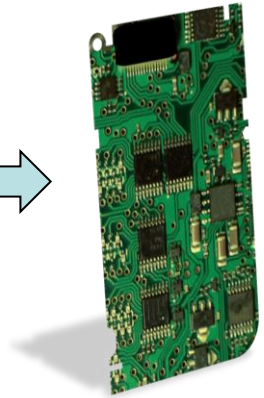
Manufacturing
Process Variation is introduced during manufacturing process (+0 mask logic process)

CP /FT Test



Product Testing
Random Noise is enhanced and generated randomly

System Assembling



System Assembling
Random Seed activates Identification, Encryption, Authentication, Security Key Storage

NeoPUF技術

- NeoPUF 的技術與設計
  - 取得隱含在製程變異中之真實亂數的創新技術
- NeoPUF提供晶片個別的獨有亂數作為IC的指紋
  - 強化晶片上資料儲存的安全性
  - 產生密碼金鑰之用
  - 作為硬體自我防護的數位簽章
  - 更多安全性防護的應用，例如安全啟動及元件信任根

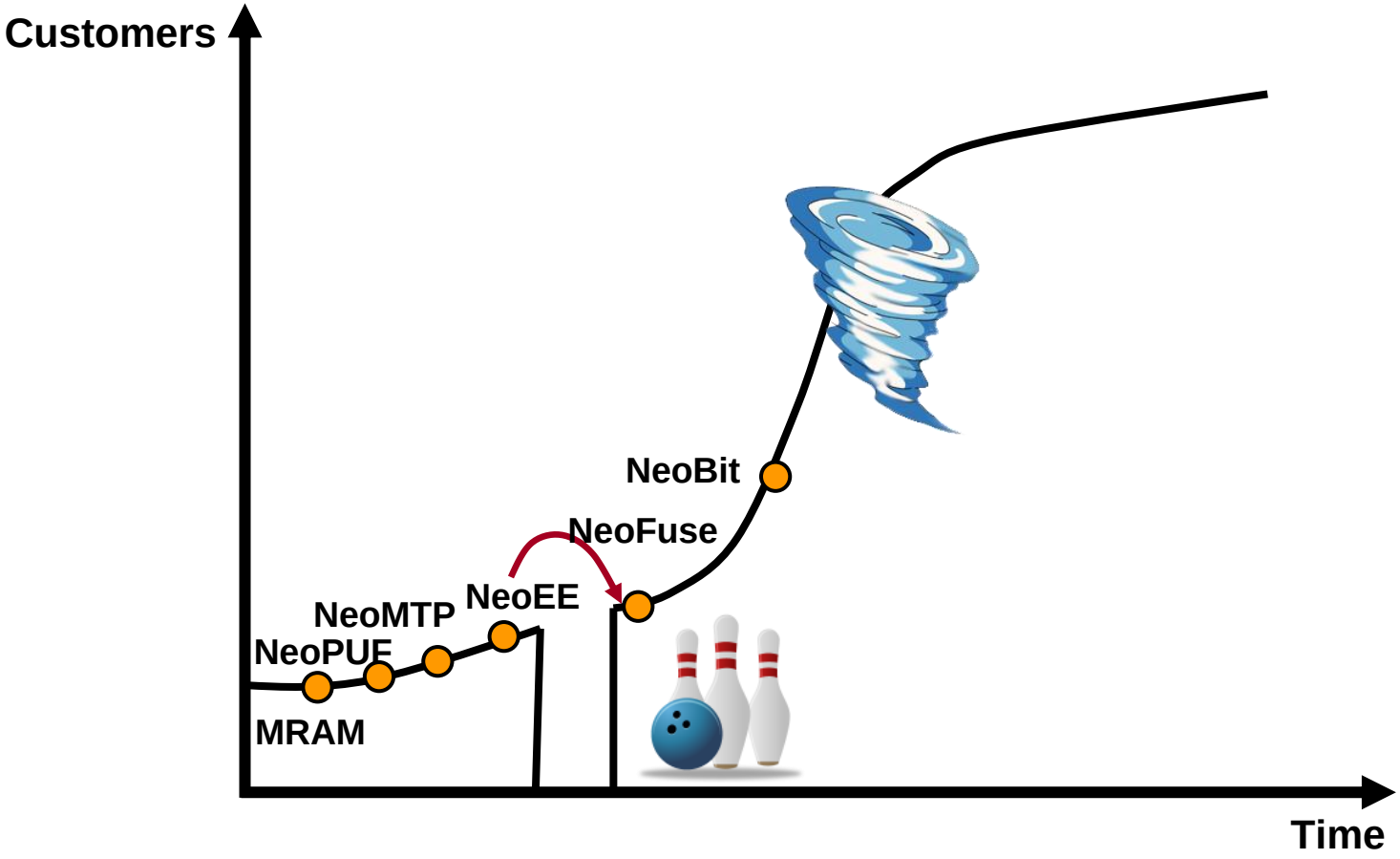
哪些應用需要NeoPUF

Device for Payment

IC with Security Data

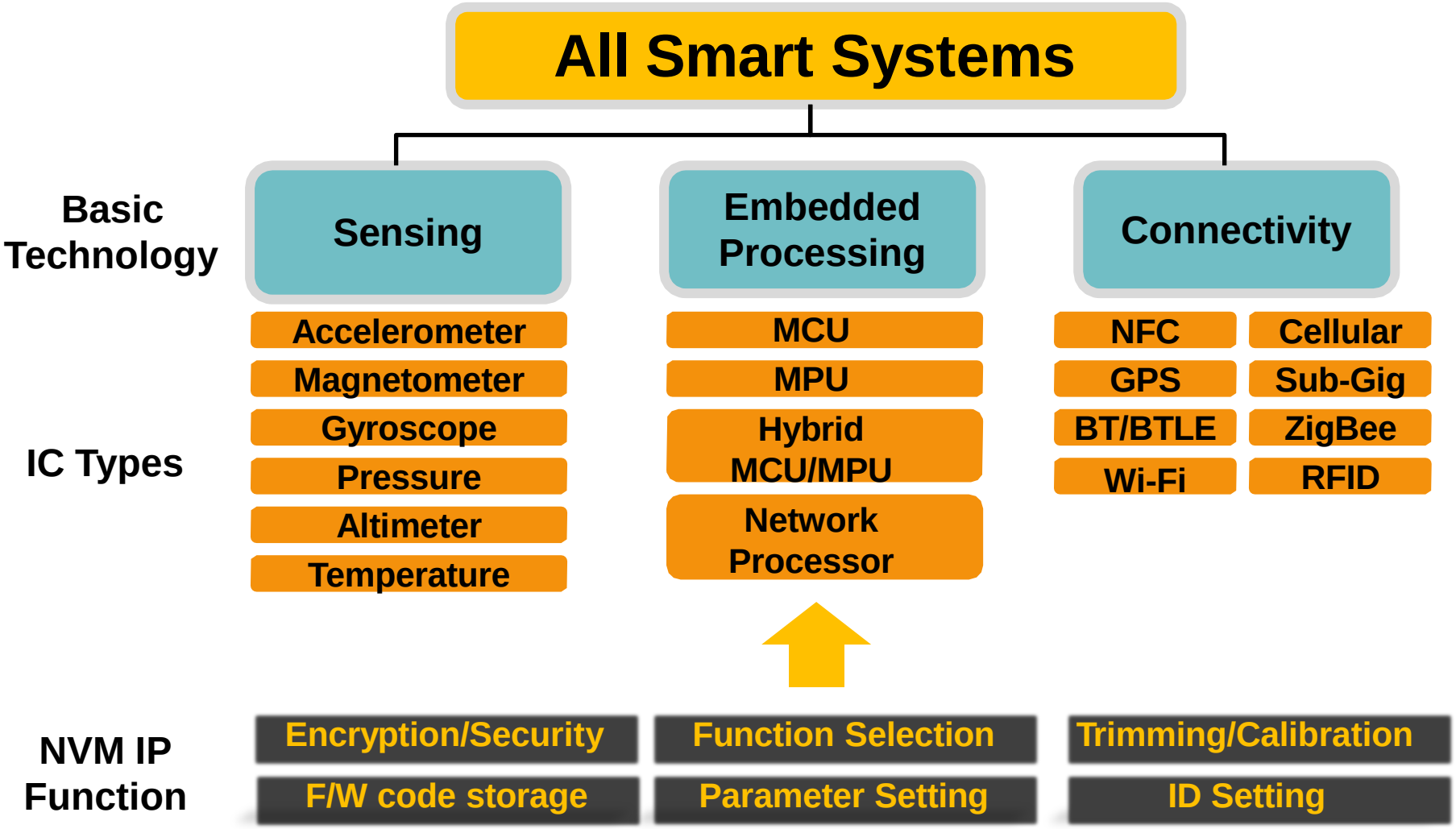
Original Device Maker

跨越鴻溝

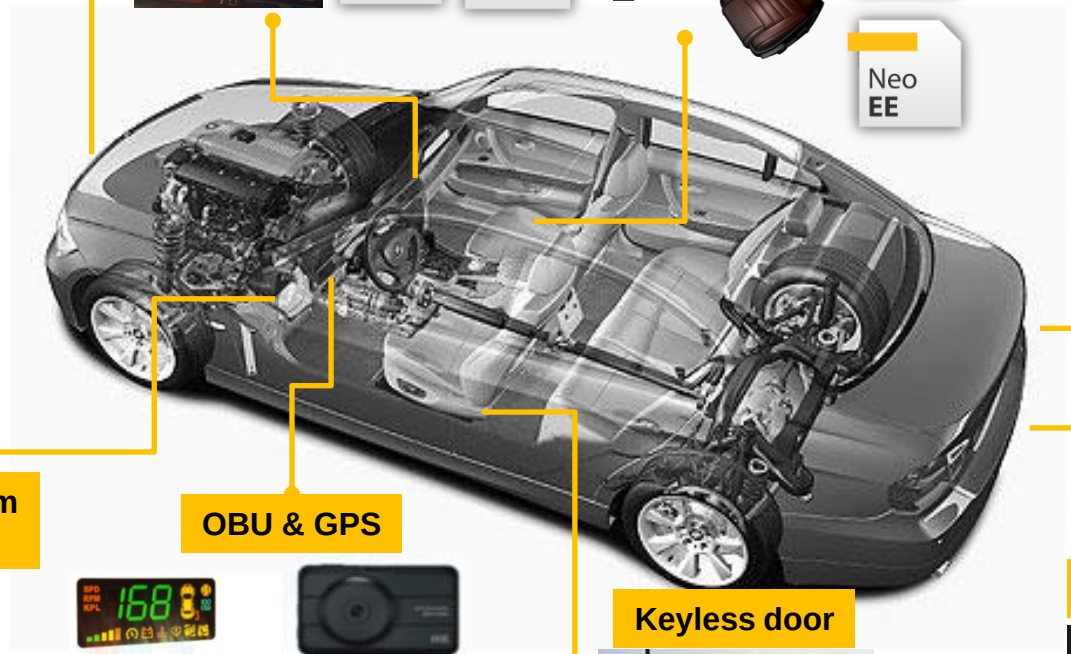


力旺矽智財引領高安全性應用

在IoT中之NVM IP 需求



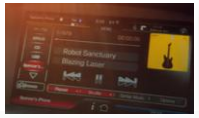
Autotronics with eMemory IPs



Intelligent drive Distronic system

Neo Bit | Neo Fuse

Infotainment system



Neo Bit | Neo Fuse

Sensor system

Neo Bit | Neo EE

Auto parking system

Neo Bit | Neo Fuse

Blind Spot Warning System Cockpit System

Neo Bit | Neo Fuse

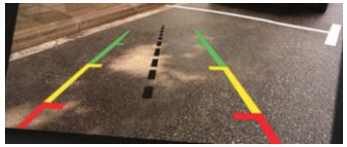
OBU & GPS

Neo Bit | Neo Fuse

Keyless door

Neo Bit | Neo EE

Rear view system



Neo Bit | Neo Fuse

未來展望

- 技術授權金：
  - 全球授權簽約之晶圓代工廠家數持續增加。
  - 力旺IP library累計技術持續增加中，也將進一步挹注設計授權金之成長動能。
- 權利金：

  <u>8吋部分</u>
  - 新一代手機應用的PMIC 內容數增加，如TypeC及Wireless Charger，且美國晶片最大客戶合約內容調整，將帶動PMIC權利金成長。
  - 我們的MTP已經獲得歐洲IDM大廠採用及準備量產。

未來展望

- 本季已有 Face ID相關tape-out。
- 車用電子的技術平台今年已開始量產。

12吋部分

- DDI的應用走向TDDI和OLED的趨勢不變。隨著TDDI和OLED應用的增加，將會貢獻12吋權利金成長。
- 機上盒、多媒體和連網相關的應用在28nm製程的設計完成定案數量持續增加，這些產品將對2018及之後的權利金作出貢獻。
- 我們的NeoFuse解決方案已經在25nm DRAM獲得採用，提供記憶體修復的功能，預期未來也將對權利金作出貢獻。

未來展望

- 技術發展
  - 我們的NeoFuse已經在7nm製程成功完成驗證。
  - 我們持續和主要晶圓廠合作開發7/12/14nm以及22nm SOI等平台的IP技術。
  - 我們已經開始與美國IDM大廠合作新興記憶體技術開發。
  - 我們的安全IP NeoPUF已經完成主要晶圓廠的驗證，今年已有客戶完成設計定案。

成長驅動力

Growth in application per mobile devices	• More chip applications per smartphone/tablet product.
Growth into more markets	• From consumer electronics and mobile devices to wearable devices. • Adding new NVM product lines further enable more product applications.
Growth in advanced technology	• Higher royalty per wafer is contributed from more advanced technology nodes.
Great IoT era	• Embedded Logic NVM will be a must.

Q & A

ememory

Embedded Wisely, Embedded Widely