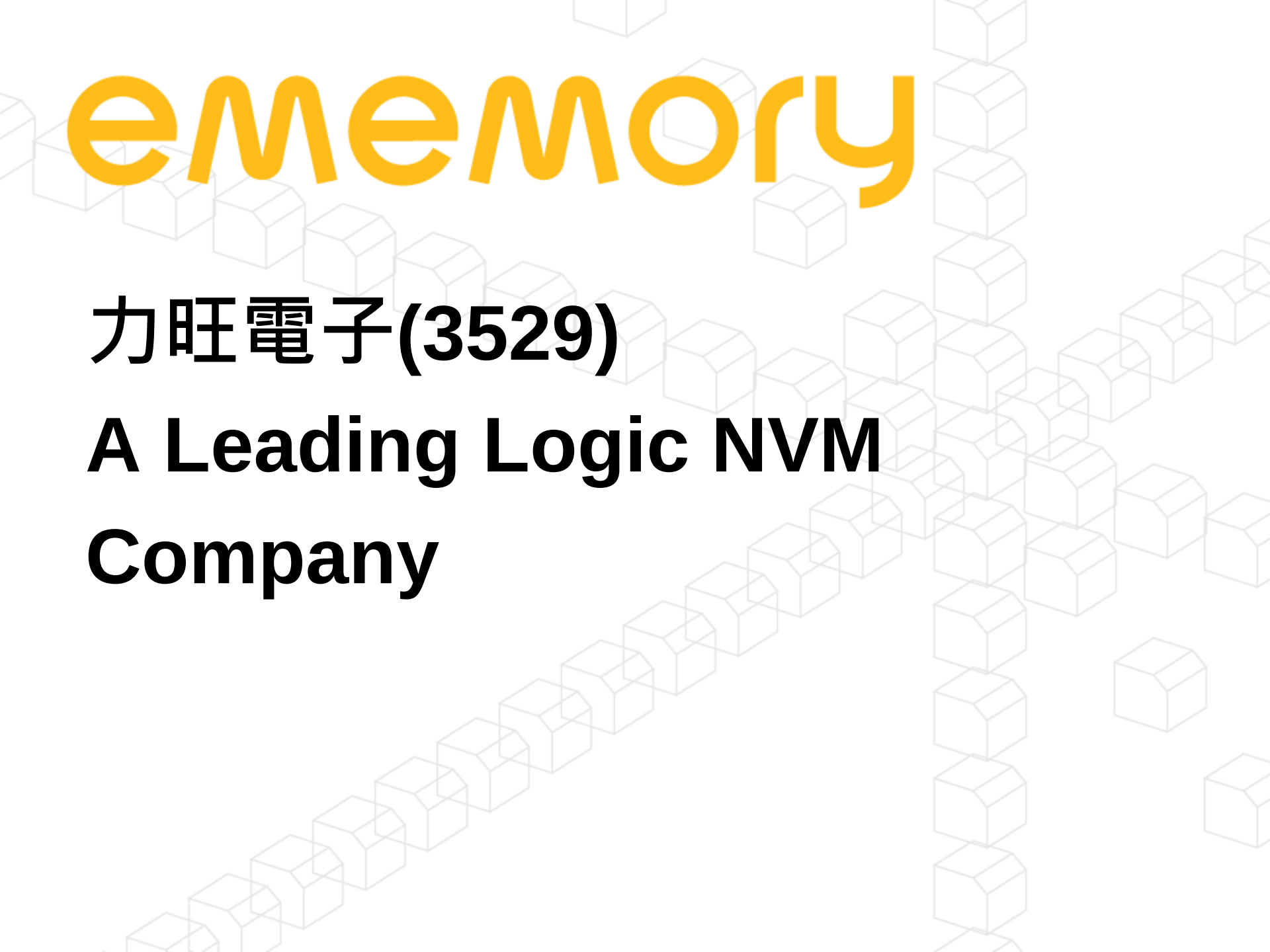


The background of the slide is white and features a pattern of numerous small, white, 3D cubes. These cubes are arranged in a way that creates a sense of depth and movement, with some cubes appearing to be stacked or falling from the top, while others are scattered across the lower half of the image. The cubes are rendered with simple black outlines and no shading, giving them a clean, geometric appearance.

ememory

力旺電子(3529)

**A Leading Logic NVM
Company**

智慧財產權聲明

本文件內之資訊，包括文字、圖片、圖表、表格或其他檔案等，其所有權利或利益，包括但不限於所有權及智慧財產權，皆屬力旺電子所有，請尊重智慧財產權。本文件之內容包含力旺電子之機密資訊。部分內容可參見 2014 年出版之 Logic Non-Volatile Memory (The NVM solutions from eMemory) 一書。任何在此之資訊在未經力旺電子書面同意，不得影印、散佈、複製、使用本文件或將其揭露予第三人。

eMemory, NeoBit, NeoFuse, NeoFlash, NeoEE, NeoMTP, NeoROM, EcoBit 與 NeoPUF 皆為力旺電子在台灣或其他國家之商標或服務標章。

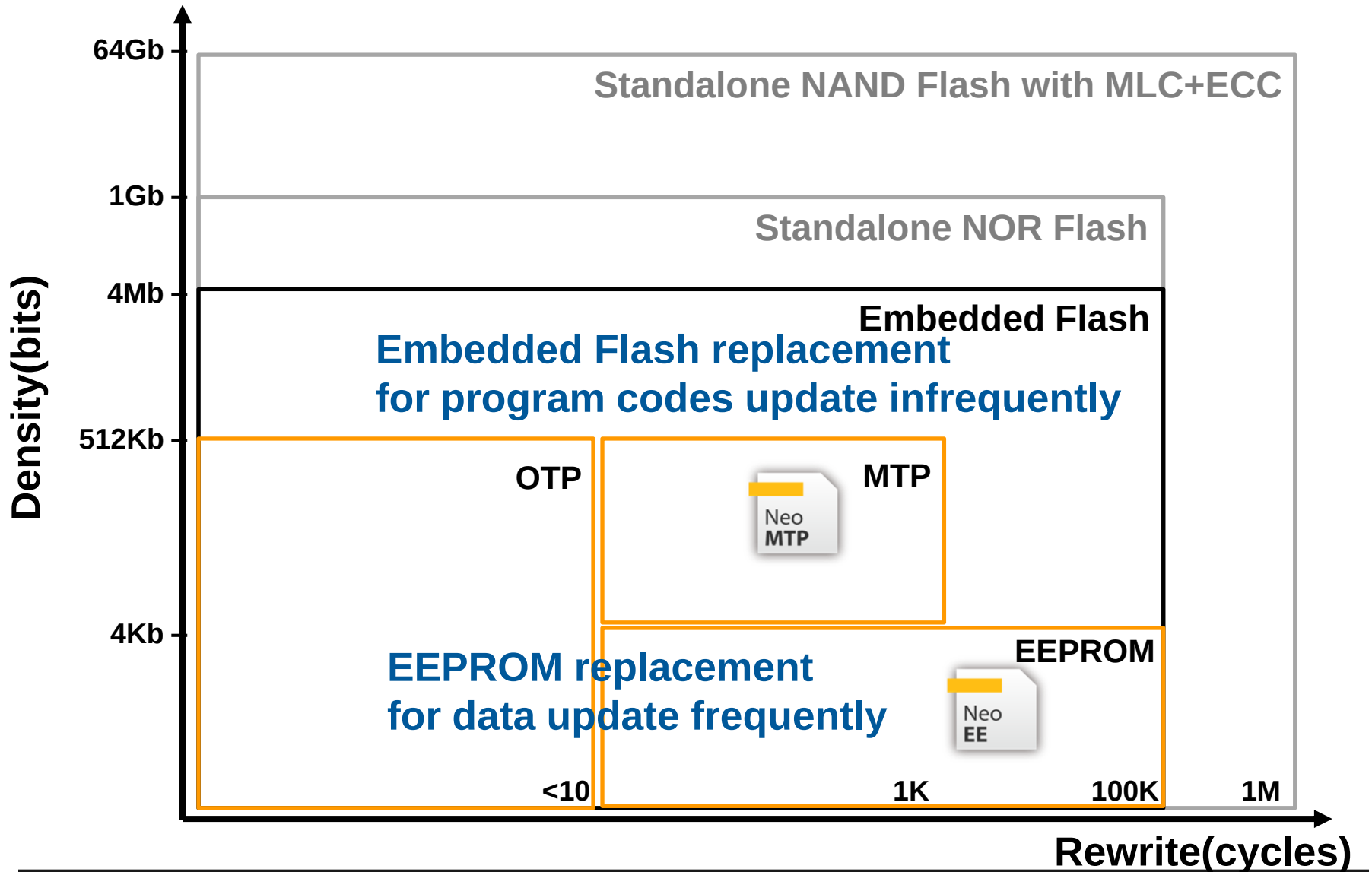
投資安全聲明

除簡報內所提供之歷史信息外，簡報事項係屬預測性陳述，受到風險及不確定性因素影響，可能造成實際結果與陳述內容發生不符，這些不確定性因素包括：技術平台是否順利導入利用、IP是否被客戶接受、客戶產品大量量產之能力及時間、產業及市場對半導體產品之供給及需求移轉、終端市場之穩定性及其他風險等。

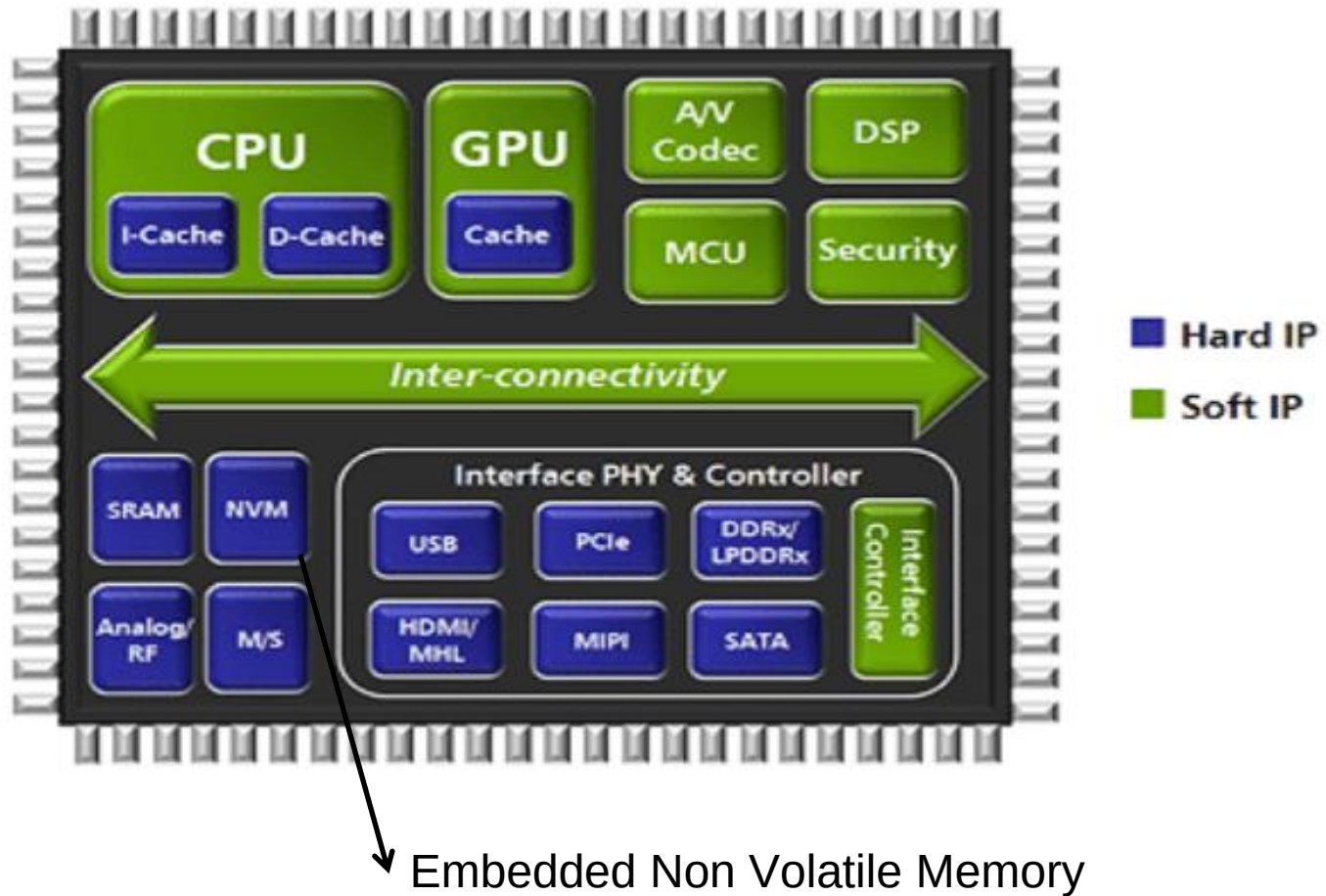
大綱

- 公司營運模式
- 營運回顧
- 成長機會與未來展望
- 問題與回答

嵌入式非揮發性記憶體分類



SOC Block Diagram



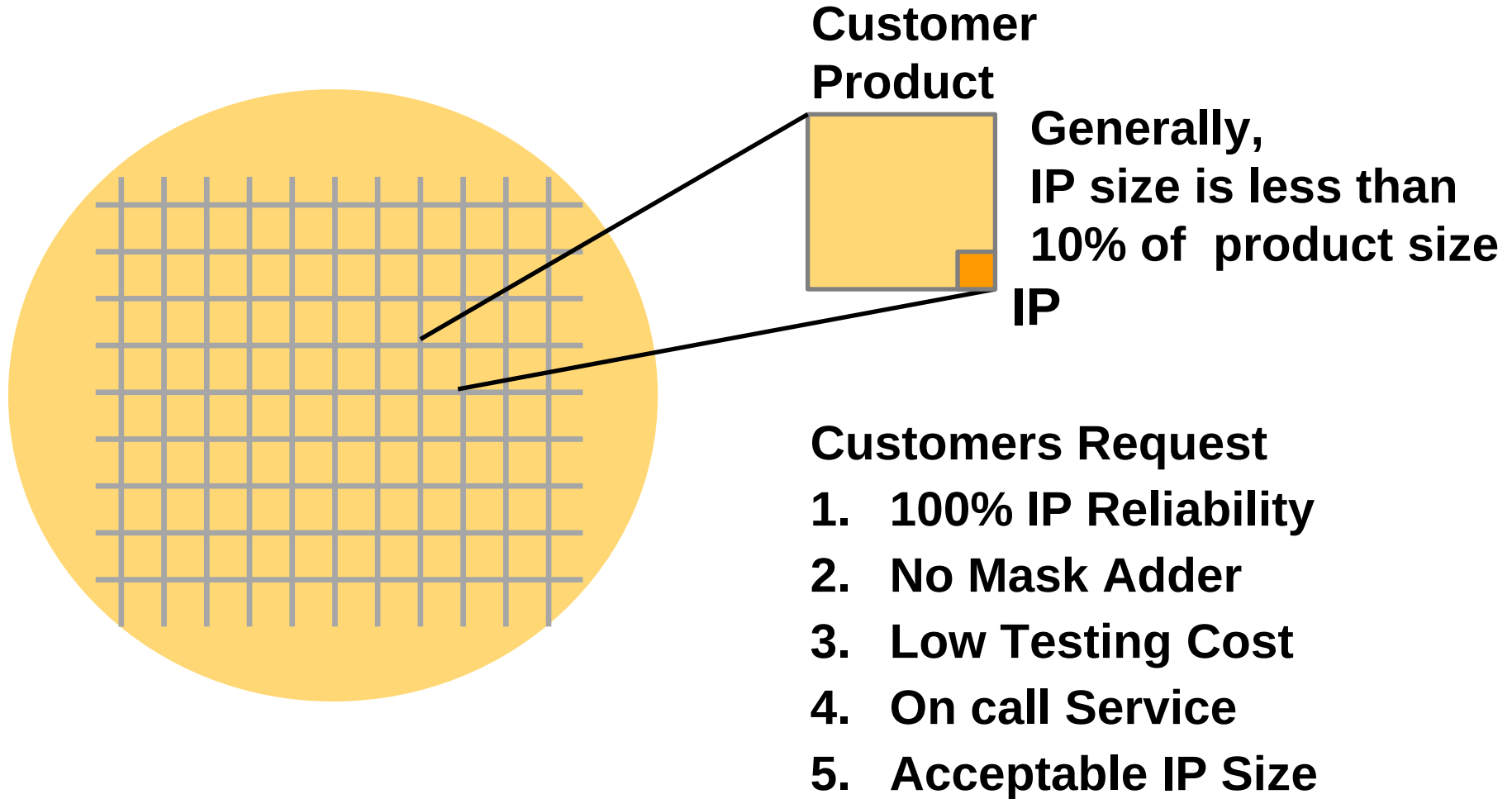
Source : tsmc

嵌入式非揮發性記憶體技術

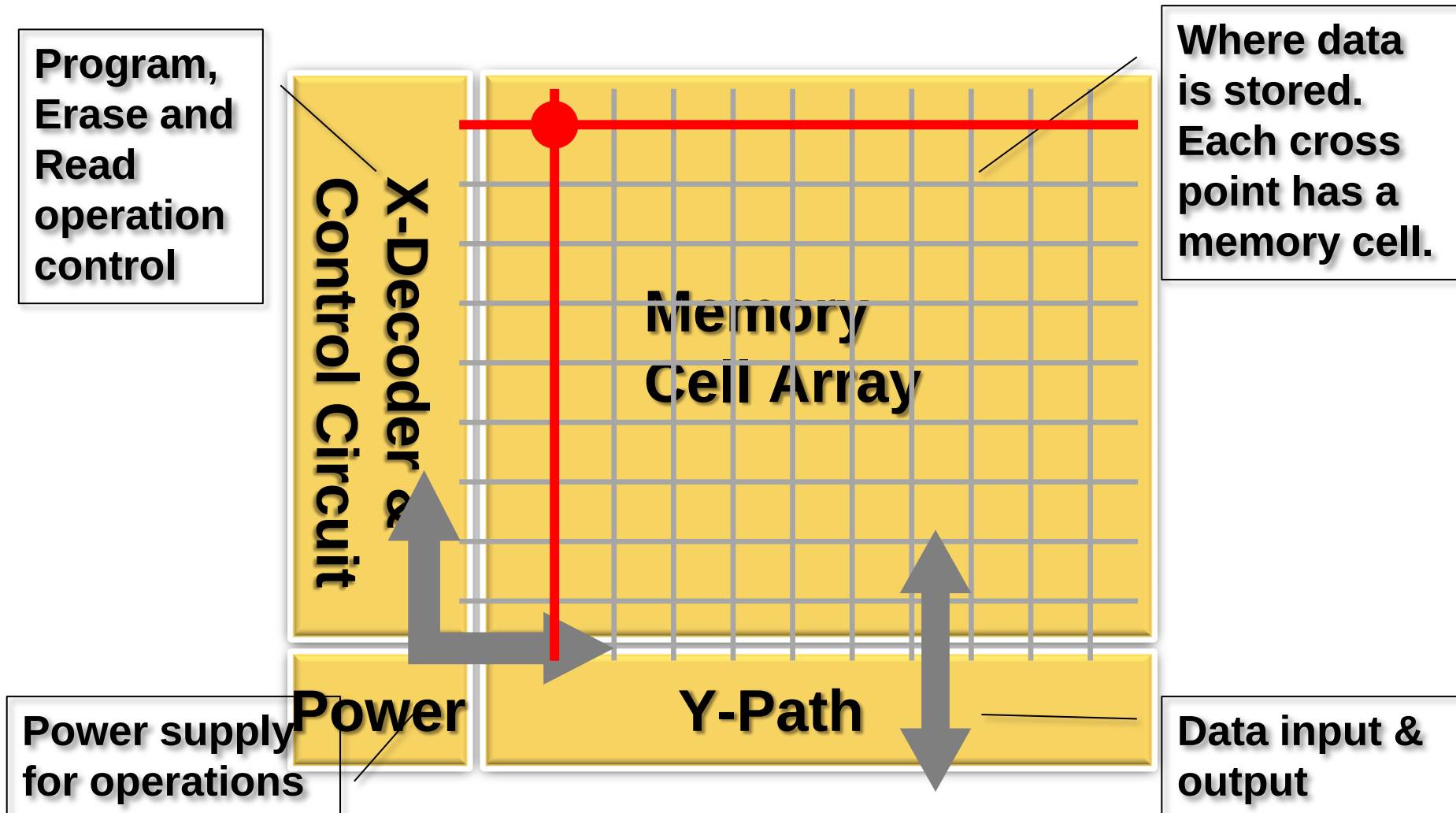
	ROM	eFuse (OTP)	Antifuse (OTP)	CMOS Floating Gate (OTP)	CMOS Floating Gate (MTP)	Embedded Flash
Cell Structure	Transistor	Poly Fuse	Antifuse	Floating Gate	Floating Gate	Floating Gate
Standard CMOS Compatible	Yes	Yes	Yes	Yes	Yes	No
Bitcell Area	< 1	50	1	2	4	1
Endurance	No	No	< 10	< 10	10K-100K	100-1000K
Density	4Kb-1Mb	256bit-4Kb	16bit-1Mb	16Kb-1Mb	1Kb-2M	64Kb-4Mb
Security	Low	Low	High	High	High	High
Additional Steps	None	None	None	None	None	+10 Mask

- ROM not programmable, eFuse cannot scale beyond 16Kb, embedded flash expensive and cannot scale after 40 nm
- eMemory's IPs: OTP (antifuse, floating gate) and MTP (floating gate)

採用IP之考量



Nonvolatile Memory IP 内部



關於力旺



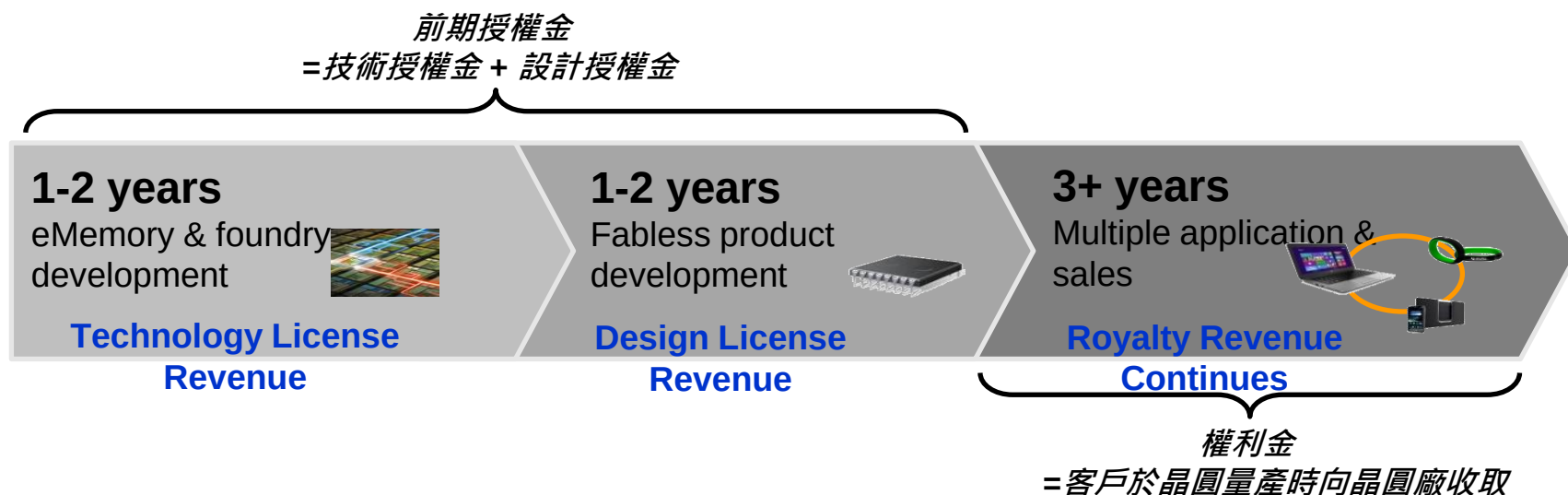
- 全世界最大的邏輯非揮發性記憶體IP公司
- 234位員工，其中161位為研發人員*
- 2011年掛牌以來，無市場籌資，無銀行借款
- 每年的現金配息率超過90%

註*: 截至 2017/06/30

營運模式

- 成長性指標:

- › 正在晶圓廠建構的製程平台數
- › 設計授權數
- › 權利金



全球客戶



	Taiwan	China	Korea	Japan	North America	Europe	Others
Foundry	5	8	3	4	1	2	1
IDM	0	0	0	8	2	1	0
Fabless	261	513	71	52	242	111	53

Foundry

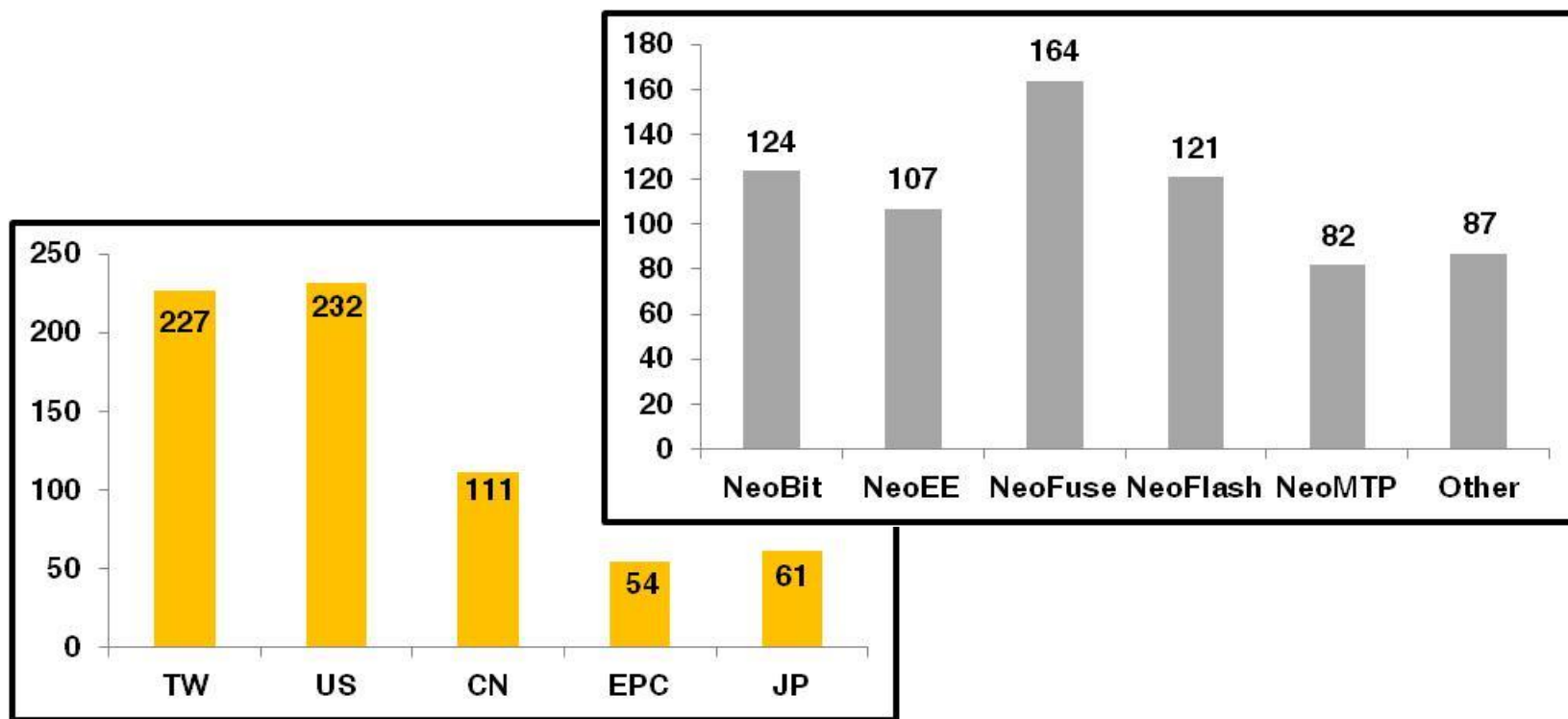


IDM



專利佈局

	1Q 17	2Q 17	Change
Pending	244	232	- 12
Issued	416	453	+ 37
Total	660	685	+ 25

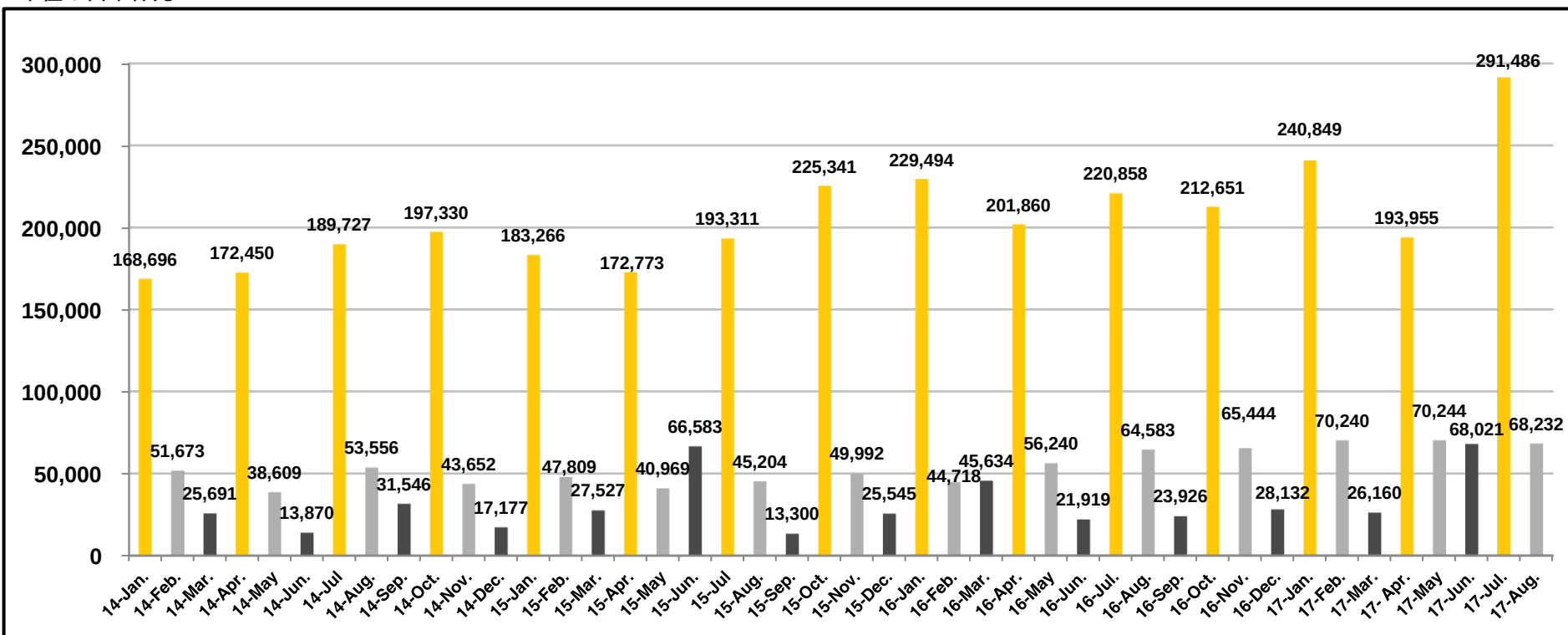


註:截至 2017/06/30

每季營收模式

- 每季第一個月認列絕大部份晶圓廠前一季使用本公司IP的出貨晶圓權利金及當月產生的技術授權金及設計授權金；第二個月則是少部份晶圓廠權利金及當月授權金；第三個月則無權利金收入，只有授權金。

單位：台幣仟元



大綱

- 公司營運模式
- 營運回顧
- 成長機會與未來展望
- 問題與回答

第二季各項營收

單位：新台幣仟元

	Q2 2017	Q1 2017	QoQ	Q2 2016	YoY	H1 2017	H1 2016	YoY
授權費	134,140	74,146	80.91%	77,715	72.61%	208,286	163,691	27.24%
權利金	198,080	263,103	-24.71%	202,304	-2.09%	461,183	436,174	5.73%
合計	332,220	337,249	-1.49%	280,019	18.64%	669,469	599,865	11.60%

單位：合約數

		Q2 2017	Q1 2017	2016	2015
技術授權數		8	5	43	28
設計 授權數	NRE	13	8	56	57
	使用費	79	88	311	349

綜合損益表

(單位:新台幣仟元)	Q2 2017	Q1 2017	Q2 2016	change (QoQ)	change (YoY)
營業收入淨額	332,220	337,249	280,019	-1.5%	18.6%
營業毛利率	100%	100%	100%	-	-
營業費用	188,562	193,603	163,276	-2.6%	15.5%
營業淨利率	43.2%	42.6%	41.7%	0.6ppts	1.5ppts
本期淨利	135,610	151,378	106,245	-10.4%	27.6%
純益率	40.8%	44.9%	37.9%	-4.1ppts	2.9ppts
每股盈餘 (單位: 新台幣元)	1.79	2.00	1.40	-10.5%	27.9%
權益報酬率	29.6%	30.2%	24.5%	-0.6ppts	5.1ppts

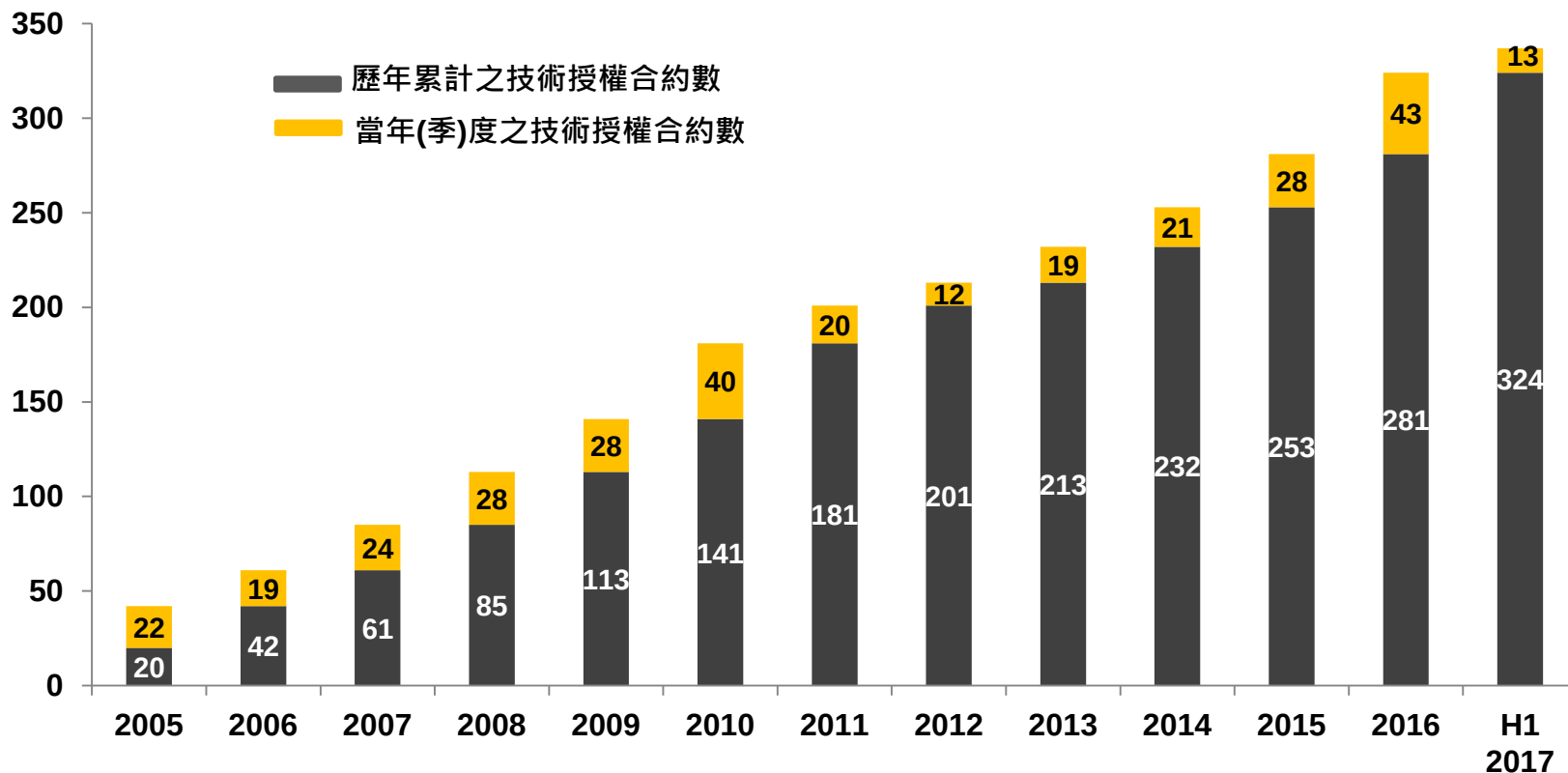
註：美金營收 QoQ成長2.2%；YoY成長26.8%

技術授權合約

單位：合約數

Year	2014	2015	2016	H1 2017
License	21	28	43	13

註：與晶圓廠簽訂的技術授權合約所含的技術製程及授權金視合約內容而定，無特別季節性因素。



目前正在建構的技術製程平台

- New technologies being developed for **104** platforms by Q2 17.
- **21** for NeoBit, **40** for NeoFuse, **20** for NeoEE, and **23** for NeoMTP.

	7/10nm	12/14/16nm	28nm	40nm	55/65nm	80/90nm	0.11~ 0.13um	0.15~ 0.18um	>0.25 um
NeoBit	-	-	-	-	-	-	8	13	
NeoFuse	3	3	8	3	10	6	4	3	-
NeoEE	-	-	-	-	-	-	3	17	-
NeoMTP	-	-	-	-	1	2	7	13	-

註: 截至 2017/06/30

目前正在建構的技術製程平台

12" Fabs	Production	Development	NVM Type	Process Type
7/10nm	0	3	OTP	FF
12/14/16nm	2	3	OTP	FF+
28nm	8	8	OTP	LP/HPM, HLP/HPM, LPS
40nm	8	3	OTP, MTP	HV-DDI, LP, eFlash
55/65nm	14	11	OTP, MTP	LP, HV-DDI, HV-OLED, DRAM, CIS, eFlash
80/90nm	6	5	OTP, MTP	HV-DDI, HV-OLED, LP, eFlash
0.13/0.11um	9	1	OTP	HV-DDI, BCD, Generic
0.18um	1	0	OTP	BCD
Total	48	34		

8" Fabs	Development	NVM Type	Process Type
90nm	3	OTP	HV-DDI, LL
0.13/0.11um	21	OTP, MTP	HV-DDI, BCD, LP, RF, CIS, LL, Green
0.18/0.16/0.152um	46	OTP, MTP	Generic, LP, LL, MR, HV, Green, BCD
0.25um	0	OTP, MTP	BCD
0.35um	0	OTP	UHV
Total	70		

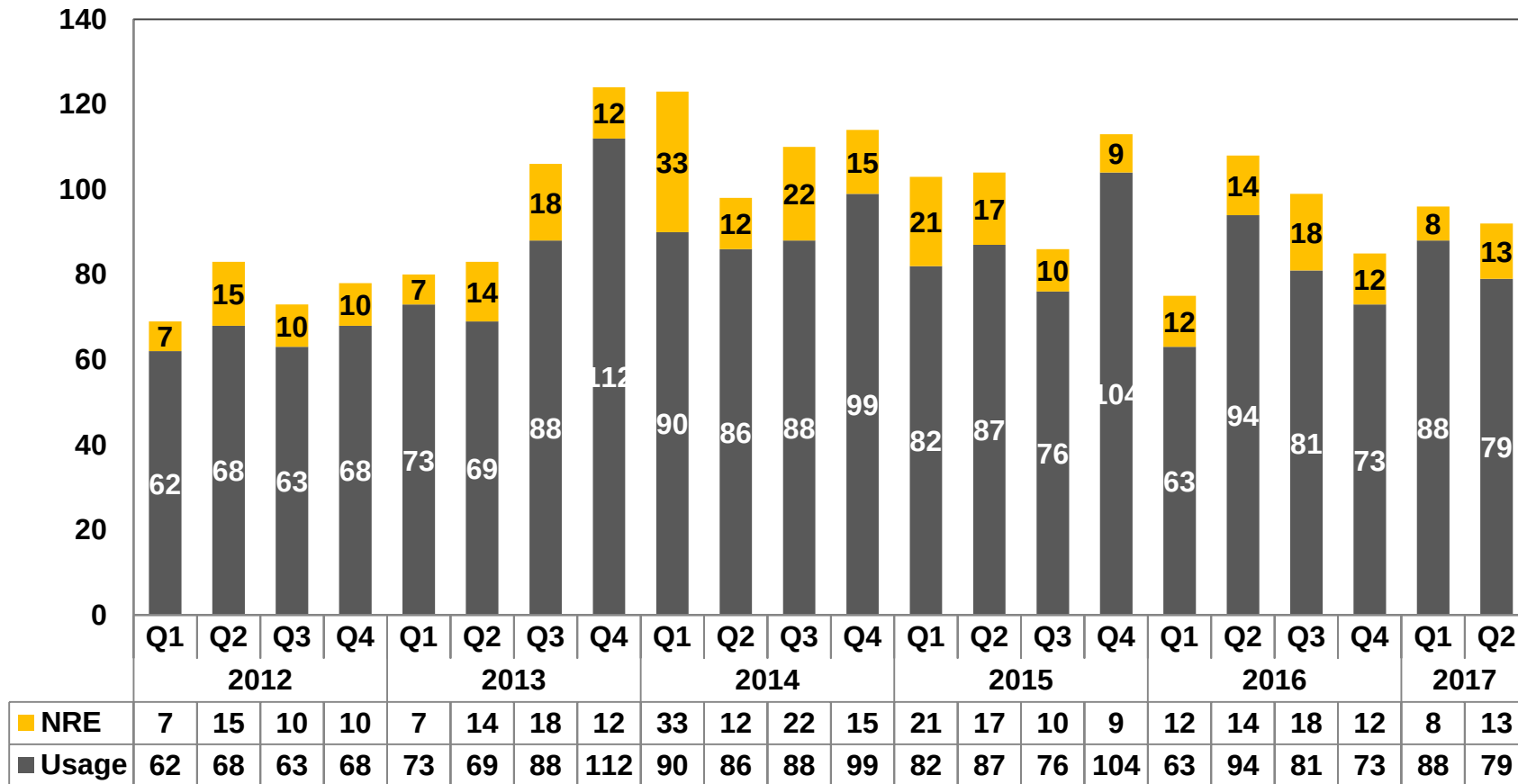
註: 截至 2017/06/30

Confidential

Embedded Wisely, Embedded Widely

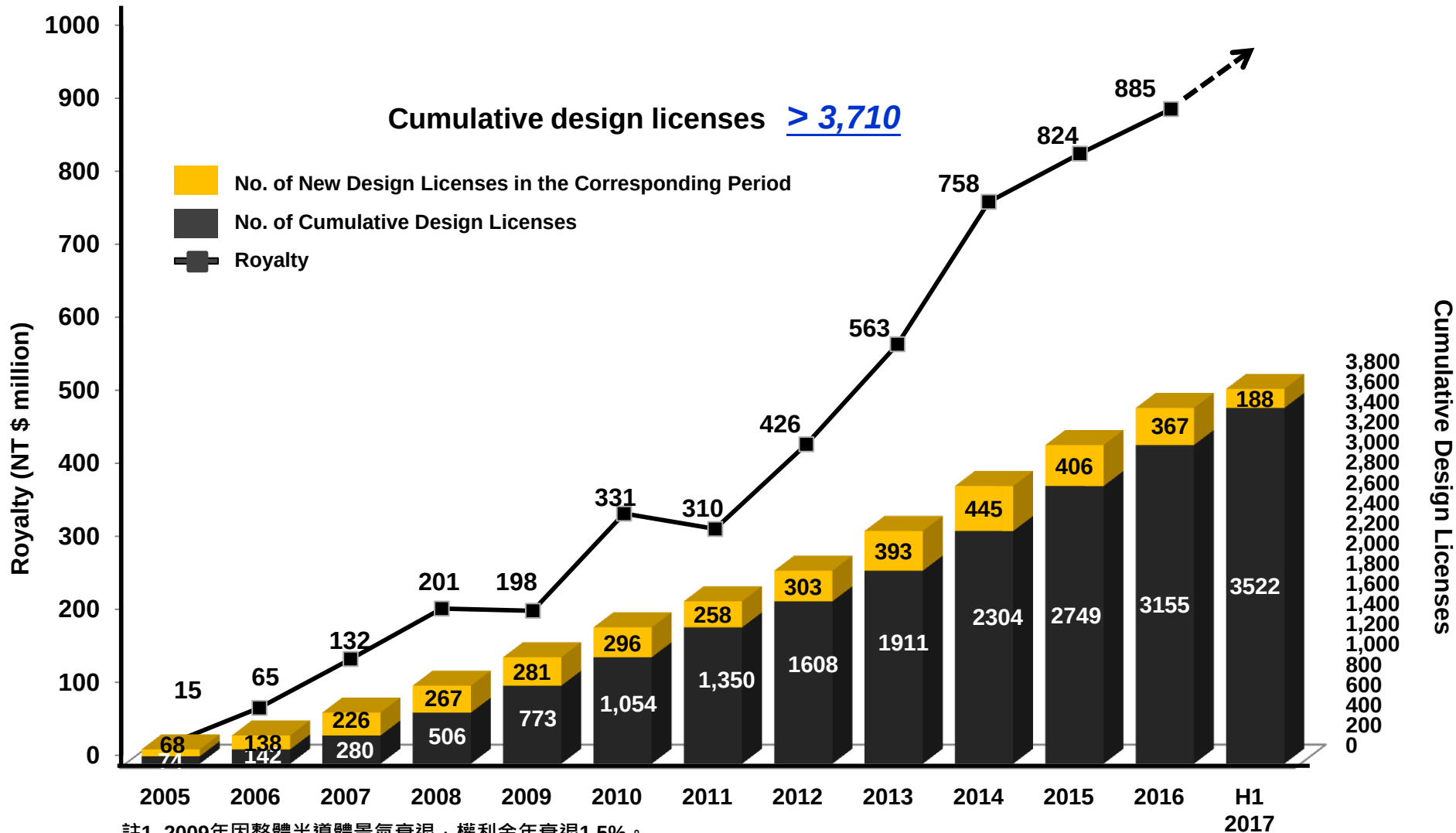
每季設計授權數(New Tape-Out)

- A total **188** NTO in H1 2017 (**367**@2016, **406**@2015, **445**@2014, **393**@2013)



註：客戶在各代工廠的諸多MCU NTO已陸續進入量產，加上與主要Green process代工廠的商業模式調整為直接license IP cell 給代工廠，由代工廠提供設計服務給客戶，造成tape out 數減少，但仍對使用IP cell 的晶片支付權利金。雖然MCU的NTO數量有明顯減少，但是相關的晶圓產出和權利金收入還是持續增加

權利金取決於過去累積的設計授權數

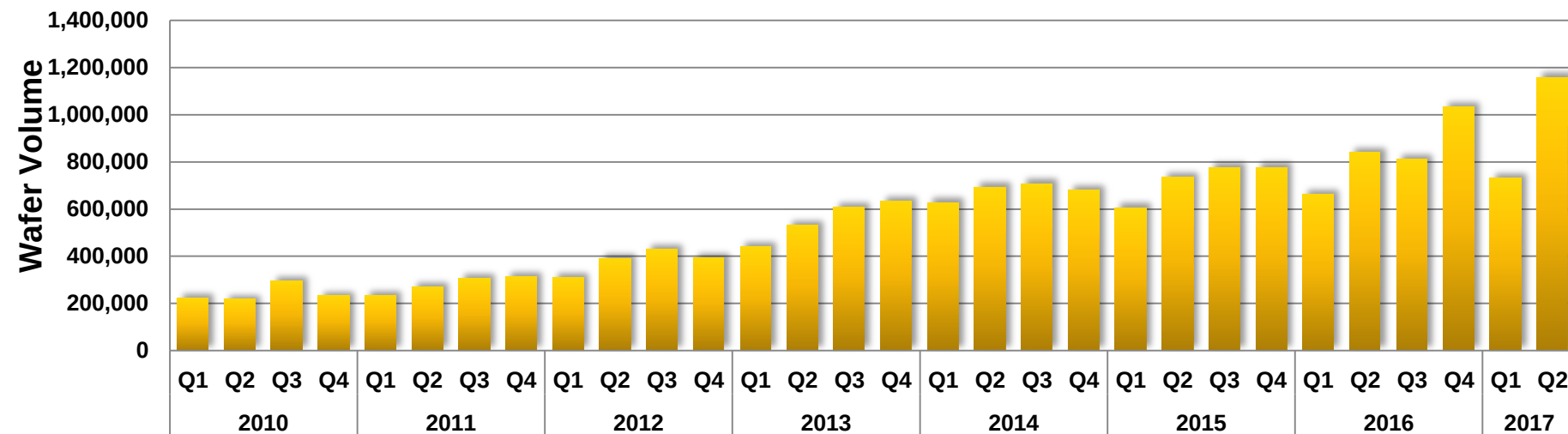


註1. 2009年因整體半導體景氣衰退，權利金年衰退1.5%。

註2. 2011年因2010年單一客戶預付權利金，導致2010年成長67%，2011年年衰退6.3%。

註3. 2009-2013年權利金年複合成長率為30%。

每季量產晶圓片數



eMemory IP's Penetration Rates in T Company (in US\$revenue)

	Process node	*% of T	Q2 17	Q1 17	2016	2015
8"	0.25/0.35	3%	44.84%	37.05%	28.15%	33.49%
	0.15/0.16/0.18	11%	7.36%*	9.10%	12.43%	8.73%
	0.11/0.13	3%	58.76%	41.92%	42.61%	29%
12"	80/90nm	5%	12.73%	10.96%	12.50%	19.85%
	55/65nm	10%	4.73%	3.50%	3.59%	0.55%
	40/45nm	13%	0%	0%	0.00%	0%
	28nm	27%	0.18%	0.56%	0.55%	0.05%
	16/20nm	26%	0%	0%	0.00%	0%
8"		18%	21.77%	16.13%	18.86%	16.64%
12"		82%	1.43%	1.15%	1.44%	1.87%
Total		100%	5.07%	3.54%	4.27%	4.76%

* T公司2017第二季營收來自各process node之比率

大綱

- 公司營運模式
- 營運回顧
- 成長機會與未來展望
- 問題與回答

力旺之NVM技術

- **Logic NVM portfolio offers one-stop-shop solution.**

- › Compatible to any process
- › Robust structure
- › Low process cost
- › Competitive macro sizes
- › Easy integration
- › Easy porting

eMemory's NVM Technology	OTP			MTP	
	NeoBit	NeoFuse	NeoFlash	NeoEE	NeoMTP
Product Type	OTP	OTP	Flash	EEPROM	MTP
Endurance (Cycles)	10	10	1K~10K	10K~100K	1K~10K
Additional Mask Steps	0	0	2-3	0	0
Technology	Floating gate	Anti-Fuse	SONOS	Floating gate	Floating gate
Scalability	Simple	Simple	Simple	Simple	Simple
Memory Density	HD < 512Kb GHD < 16Mb	< 4Mb	< 2Mb	< 4Kb	< 512Kb

力旺IP的應用

12"							8"			
7nm	10nm	12/14/16nm	28nm	40nm	55/65nm	80/90nm	110/130nm	160/180nm	250nm	350nm

NeoBit

NeoFuse

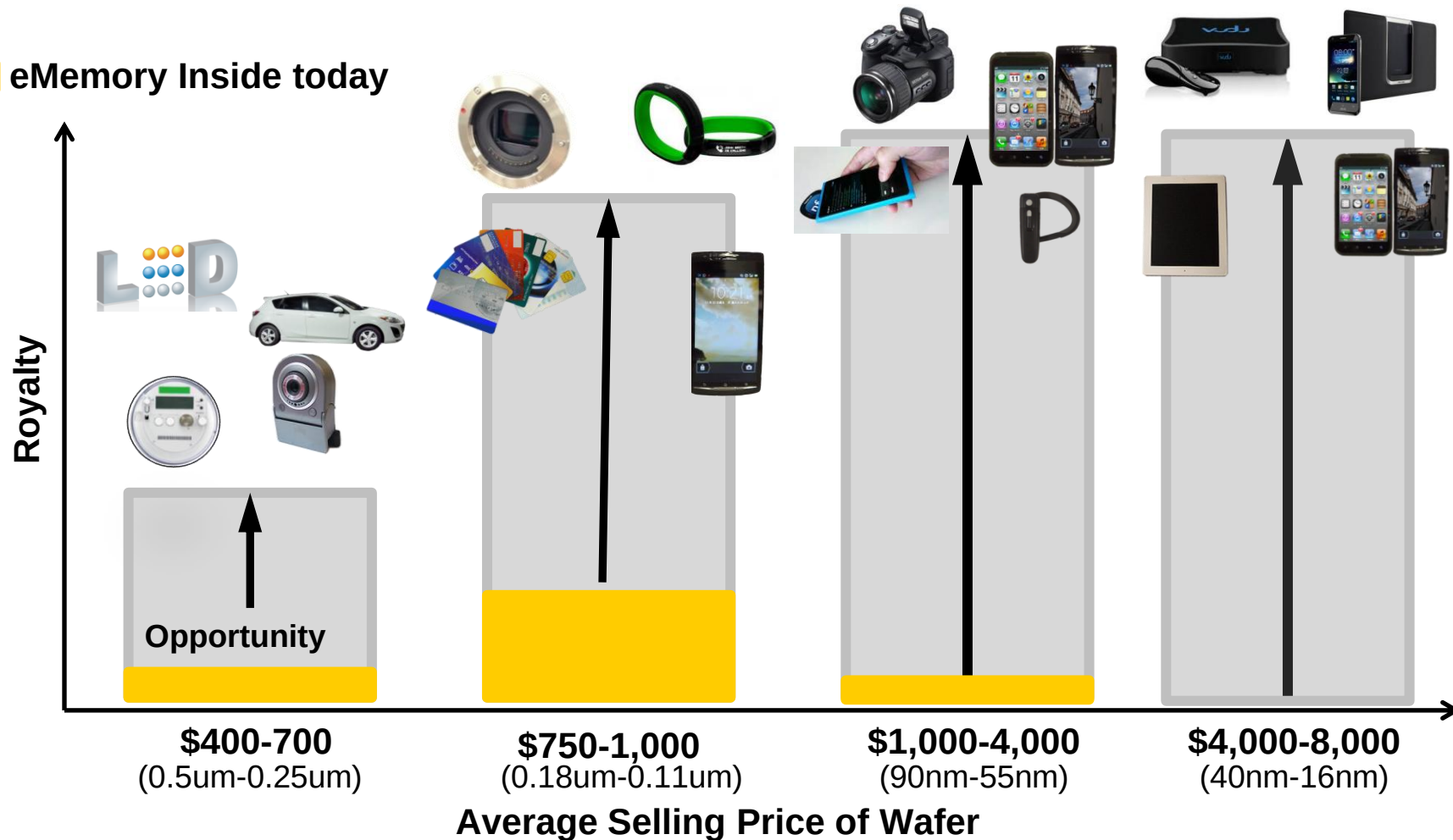
NeoFlash

NeoEE

NeoMTP

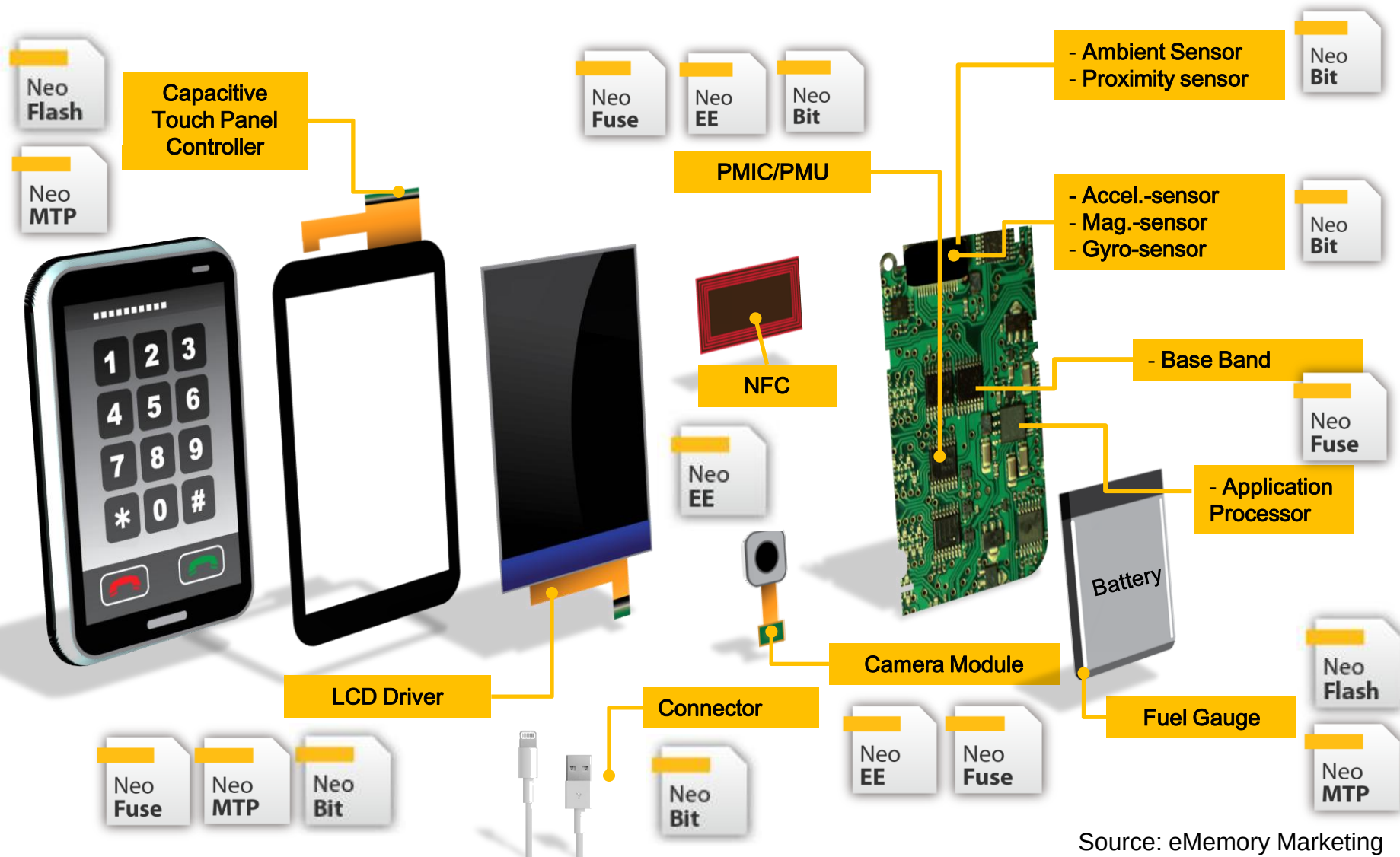
商機與潛力

■ eMemory Inside today



Note: 2.2 million 8" equivalent wafers with eMemory IP were shipped in 2013. (~5% of WW foundry shipment)

智慧型手機中力旺 IP 的應用



Source: eMemory Marketing

Benefits from Using eMemory IPs

Design-in for

1. Trimming
2. Parameter Setting
3. Code Storage
4. Identification Setting
5. Encryption
6. Function Selection

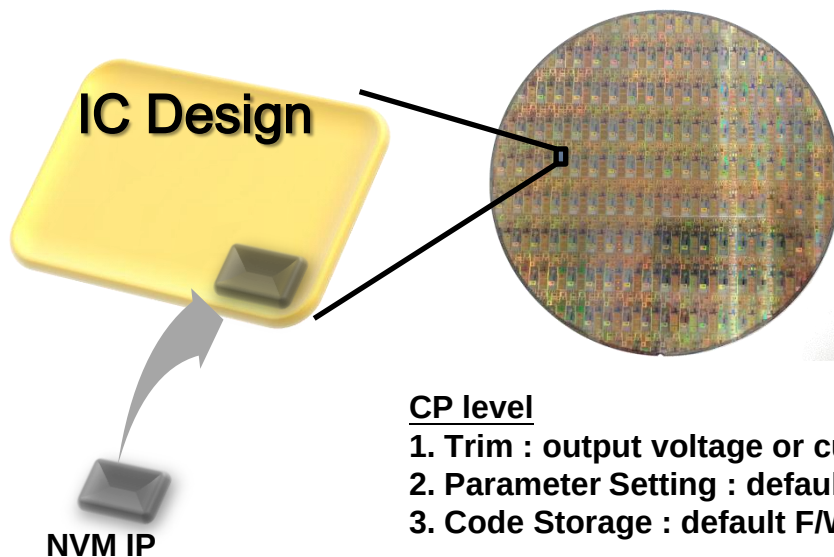
Package/FT level

1. Trim : SPEC shift
2. Parameter Setting : cross chip optimization
3. Identification Setting : manufacturer resume
4. Function Selection : setting for target market

CP Test

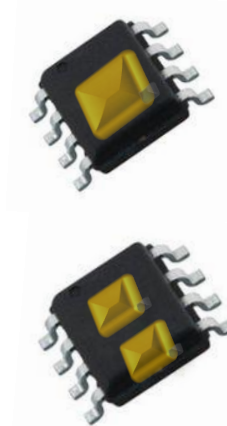
Package/FT

System Assembling



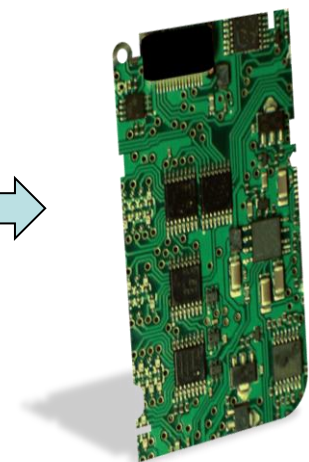
CP level

1. Trim : output voltage or current
2. Parameter Setting : default value
3. Code Storage : default F/W code



System Assembling

1. Parameter Setting : cross chip optimization
2. Code Storage : F/W code modification
3. Identification Setting : manufacturer resume
4. Encryption : Security algorithm or key storage



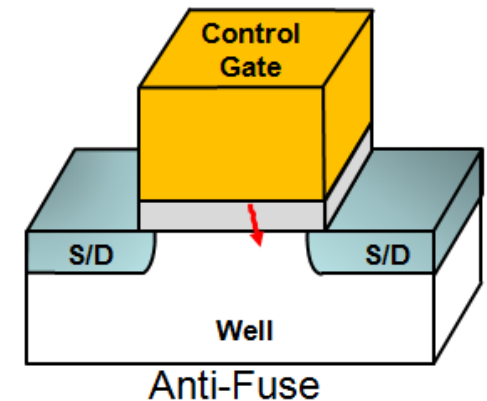
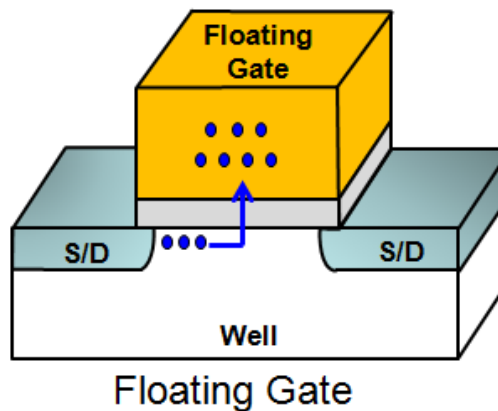
高機密性的安全設定

- Provide “Invisible Hardware Key” for invisible storage
- Prevent reverse-engineering to detect content of security key
- Protect firmware and hardware of ICs from pirating
- Extend & protect customer’s business

eFuse Key: Data is easily observed



Invisible Hardware Key : Data is hard to be detected



硬體設計防護

Authorized Product



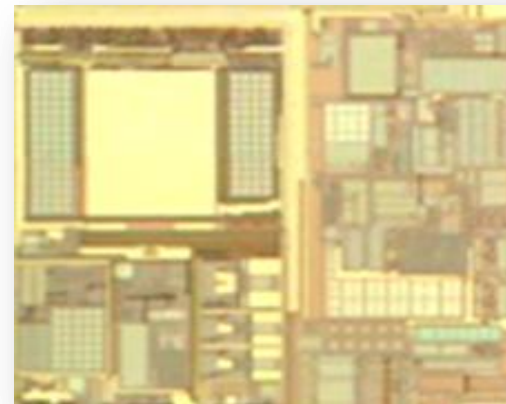
reverse
copy

re-produce



without protection

Fake Product



reverse
copy

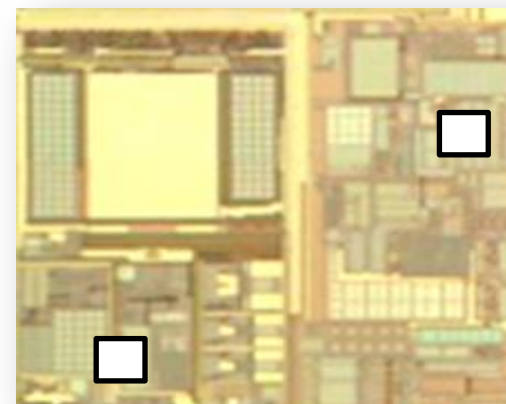
re-produce



with protection

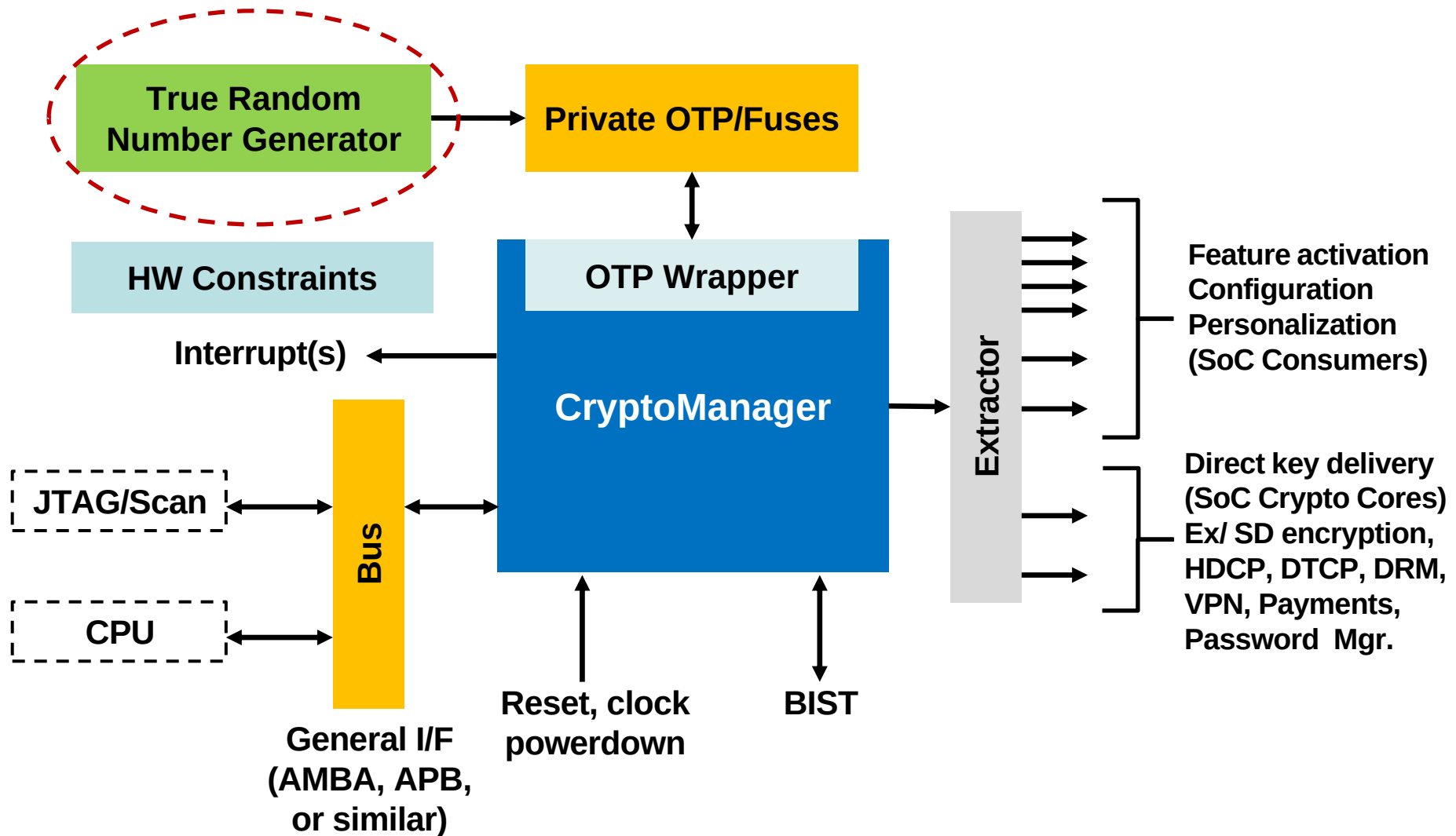


Security IP/Code by
Authorized Use



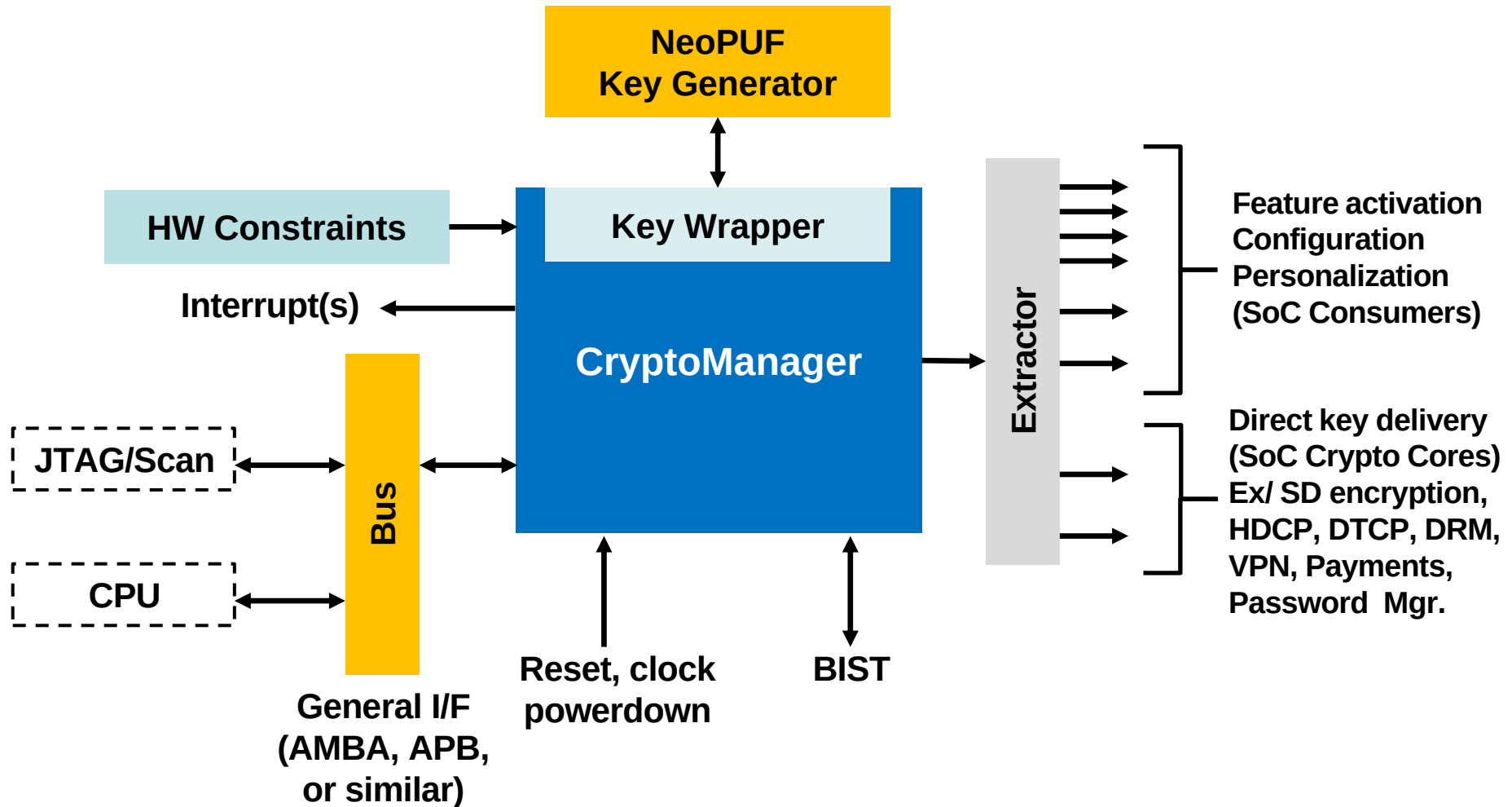
Can NOT Work w/o
Security IP/Code

OTP在加密儲存應用



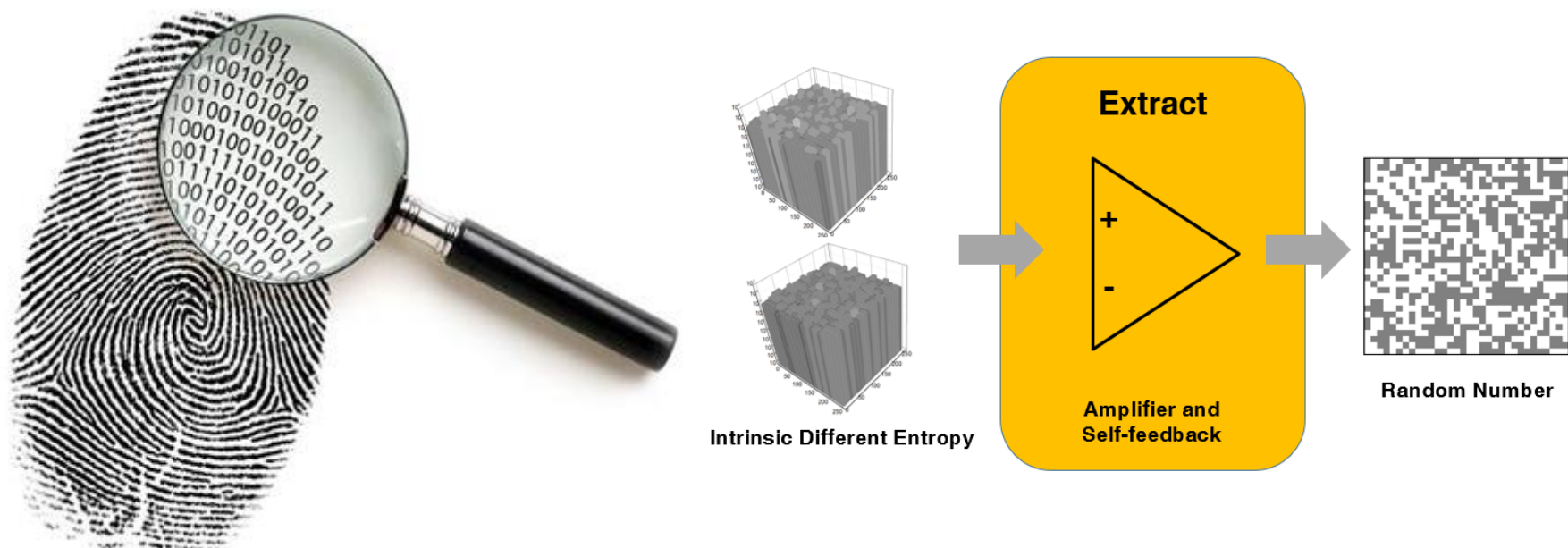
Source : Rambus crypto manager platform

NeoPUF在加密金鑰的應用



Source : Rambus crypto manager platform

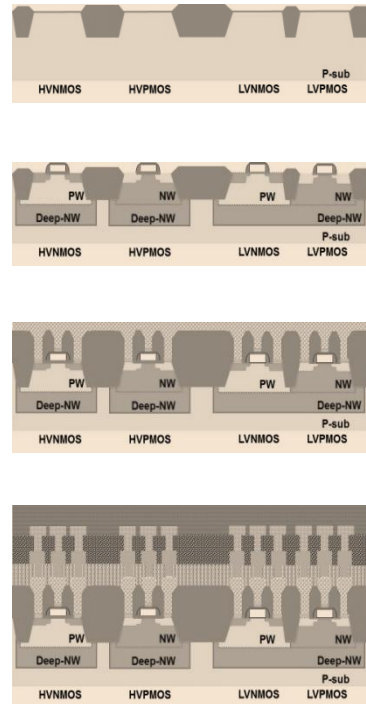
何為 PUF (P_{hysical} U_{nclonable} F_{unctions})



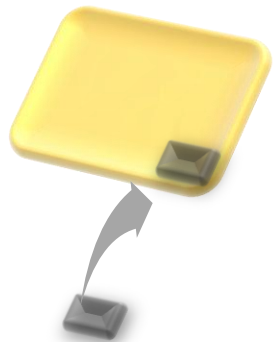
Collision Probability $\doteq 1/15B \doteq 1/2^{34}$ Collision Probability = $1/2^{\text{Bits Stream Length}}$

NeoPUF技術

Wafer Process



IC Design

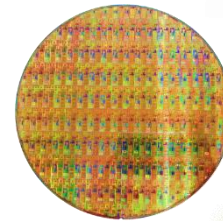


eMemory IP

Design-in
Customized SPEC & Function are designed for customer demands

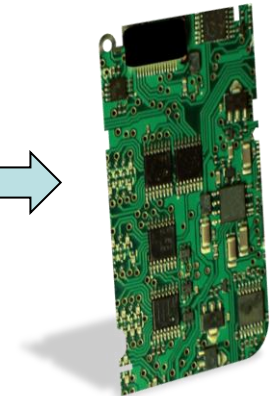
Manufacturing
Process Variation is introduced during manufacturing process (+0 mask logic process)

CP /FT Test



Product Testing
Random Noise is enhanced and generated randomly

System Assembling



System Assembling
Random Seed activates Identification, Encryption, Authentication, Security Key Storage

NeoPUF技術

- NeoPUF 的技術與設計

- › 取得隱含在製程變異中之真實亂數的創新技術

- NeoPUF提供晶片個別的獨有亂數作為IC的指紋

- › 強化晶片上資料儲存的安全性

- › 產生密碼金鑰之用

- › 作為硬體自我防護的數位簽章

- › 更多安全性防護的應用，例如安全啟動及元件信任根

哪些應用需要NeoPUF



Device for Payment

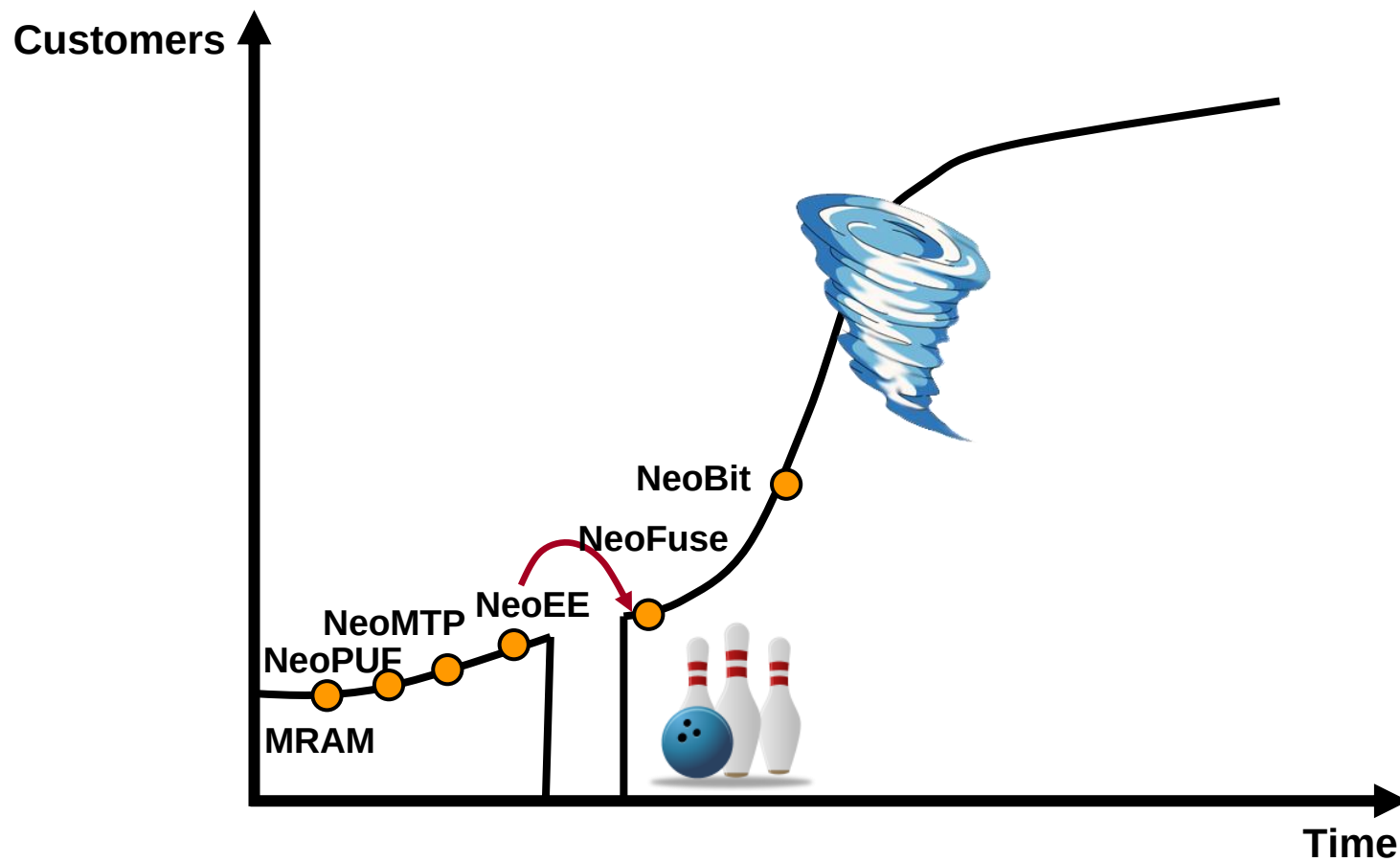


IC with Security Data



Original Device Maker

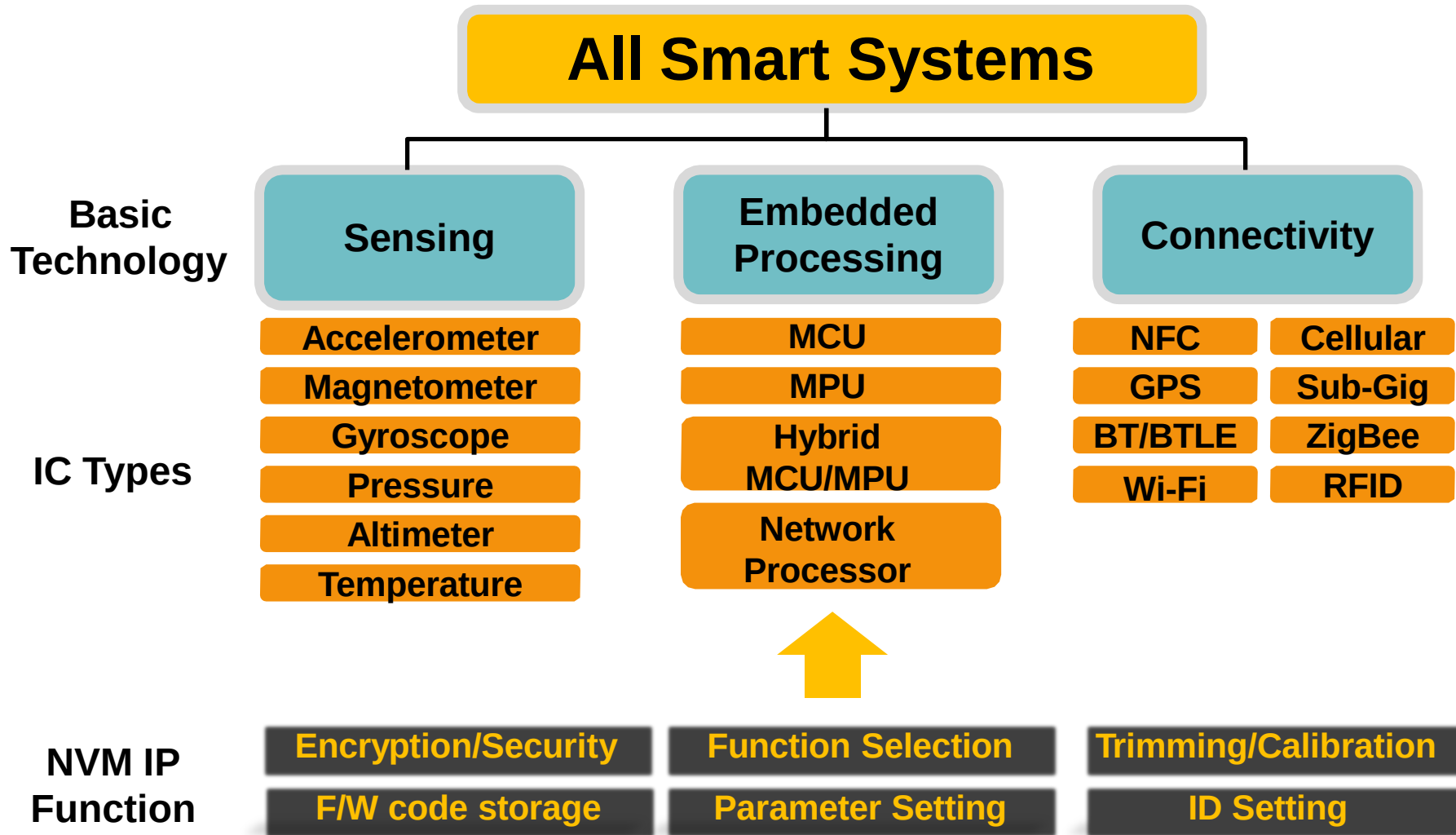
跨越鴻溝



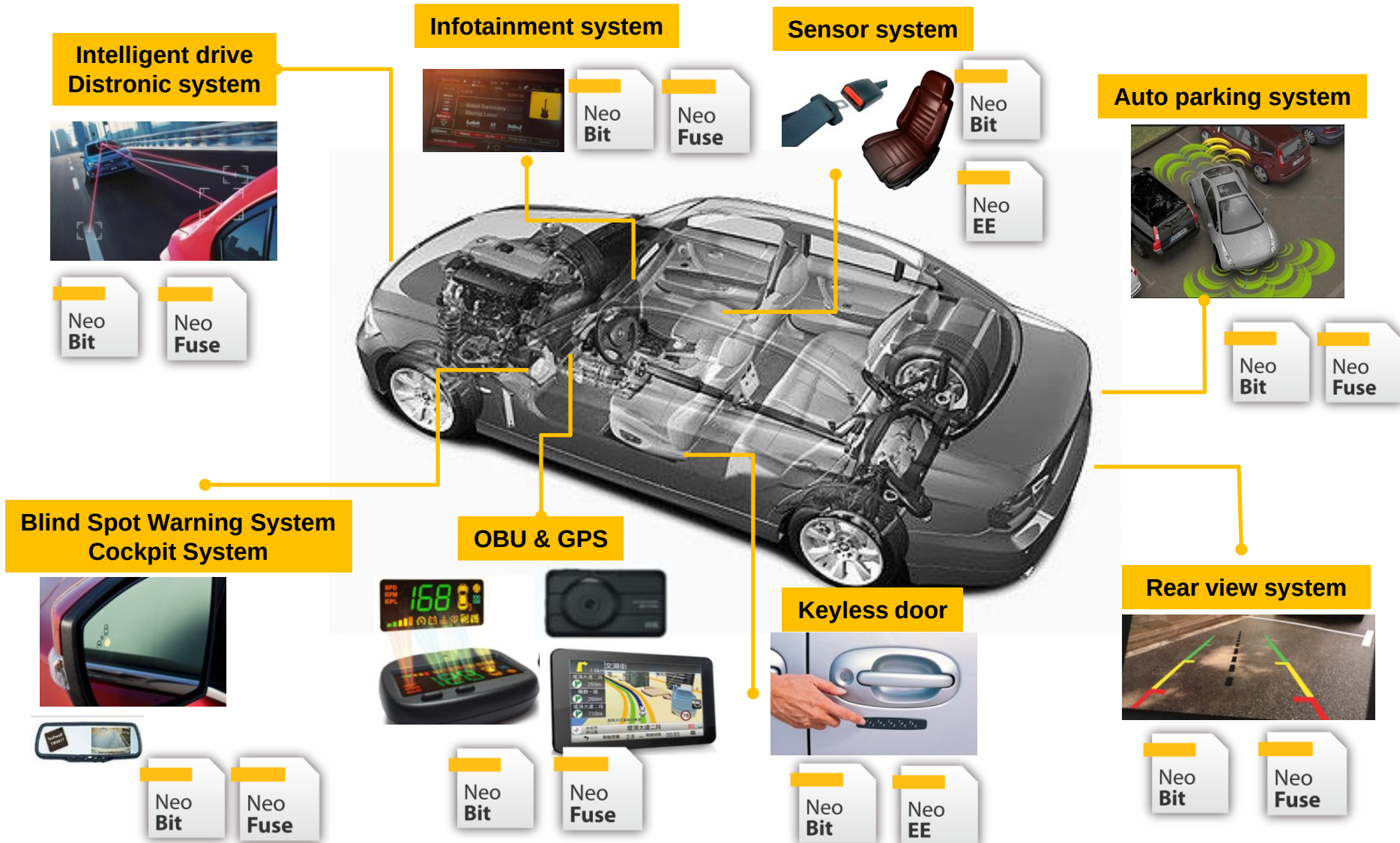
力旺矽智財引領高安全性應用



在IoT中之NVM IP 需求



Autotronics with eMemory IPs



未來展望

預期下半年營收的成長動能將會持續加速，原因如下：

- 技術授權金：

- › 全球授權簽約之晶圓代工廠家數持續增加。
- › 各大晶圓代工廠持續開發先進製程及MTP平台，技術授權金及設計授權金可望持續成長。
- › 力旺IP library累計技術持續增加中，也將進一步挹注設計授權金之成長動能。

- 權利金：

- 8吋晶圓

- › 指紋辨識IC持續呈現爆發性成長，應用層面從高階手機擴大到中低階手機。隨著更多Fingerprint客戶導入量產，權利金貢獻將顯著增加。

未來展望

- ▶ 新一代手機**PMIC** 內容數增加，下半年美國手機客戶新產品進入量產，來自**PMIC**的權利金會明顯回升；此外，美國晶片最大客戶合約內容調整，也將帶動**PMIC**權利金大幅提升。
- ▶ **MTP**系列**IP**逐漸導入設計，亦將增添權利金的成長動能。
- ▶ 車用相關應用也開始挹注權利金營收。

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- ▶ 面板技術逐漸轉移至**TDDI**及**OLED**，客戶高階**TDDI (55nm)**及**OLED (40nm)**應用持續量產，將為權利金成長帶來貢獻。
- ▶ **STB**、**Multimedia**及**Network** 等相關應用持續於**28奈米**以下先進製程**tape-out**新產品，可望為權利金成長帶來更多動能。

未來展望

- 技術研發：

- › 12奈米及22奈米SOI IP已經tape out；7奈米的IP順利在4月份tape-out，9月份將在另一代工廠tape-out。
- › 加密相關的新技術 - NeoPUF已通過主要代工廠的驗證，今年會有客戶導入設計。
- › 車用電子的技術平台今年已開始量產。

成長驅動力

Growth in application per mobile devices

- More chip applications per smartphone/tablet product.

Growth into more markets

- From consumer electronics and mobile devices to wearable devices.
- Adding new NVM product lines further enable more product applications.

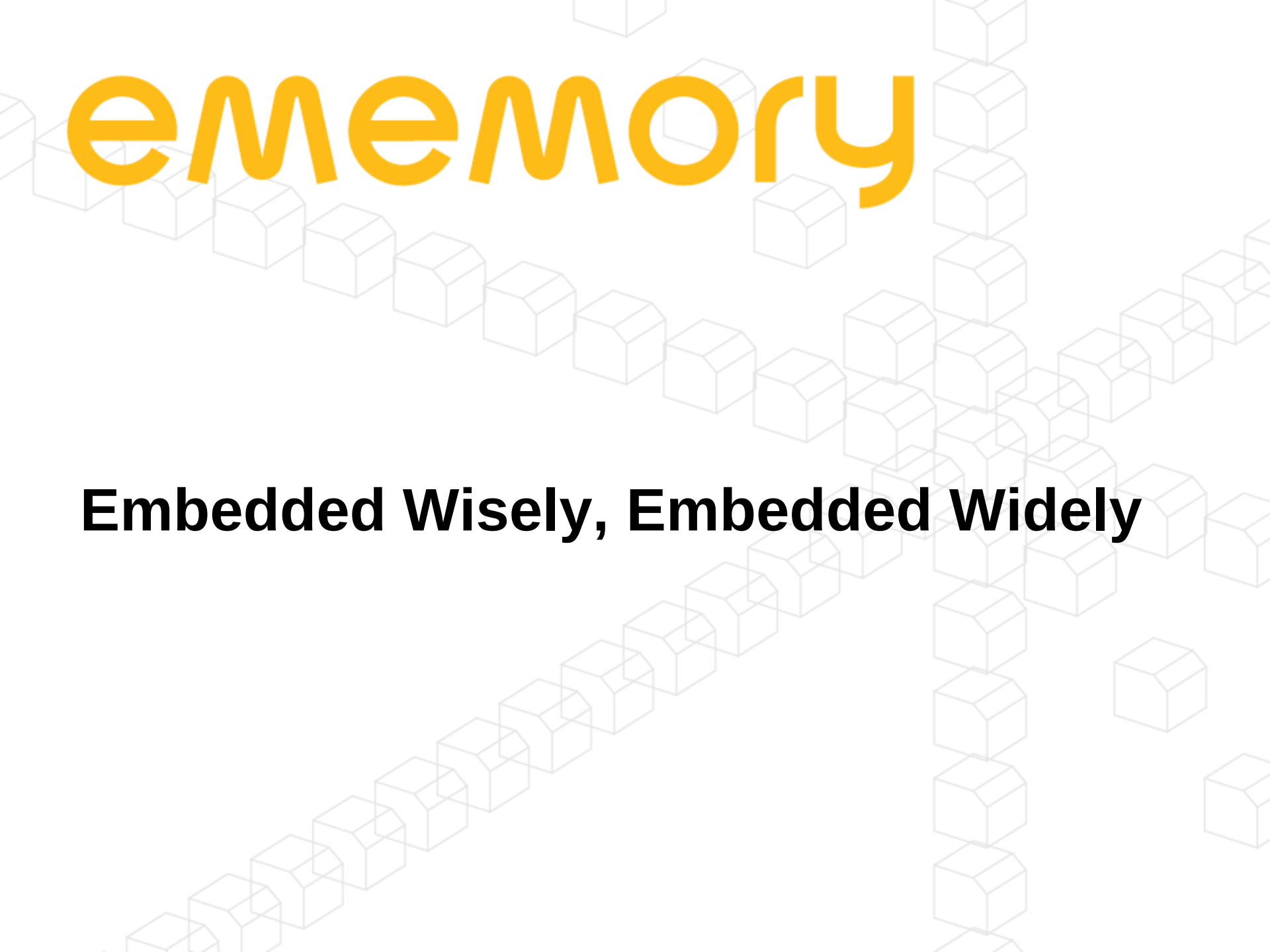
Growth in advanced technology

- Higher royalty per wafer is contributed from more advanced technology nodes.

Great IoT era

- Embedded Logic NVM will be a must.

Q & A



ememory

Embedded Wisely, Embedded Widely