A Leading Logic NVM Company
IPR Notice

All rights, titles and interests contained in this information, texts, images, figures, tables or other files herein, including, but not limited to, its ownership and the intellectual property rights, are reserved to eMemory. This information may contain privileged and confidential information. Some contents in this information can be found in Logic Non-Volatile Memory (The NVM solutions from eMemory), published in 2014. Any and all information provided herein shall not be disclosed, copied, distributed, reproduced or used in whole or in part without prior written permission of eMemory Technology Inc.

eMemory, NeoBit, NeoFuse, NeoFlash, NeoEE, NeoMTP, NeoROM, EcoBit and NeoPUF are all trademarks and/or service marks of eMemory in Taiwan and/or in other countries.
Cautionary Statement

This presentation contains forward-looking statements, which are subject to risk factors associated with semiconductor and intellectual property business. It is believed that the expectations reflected in these statements are reasonable. But they may be affected by a variety of variables, many of which are beyond our control. These variables could cause actual results or trends to differ materially which include, but are not limited to: wafer price fluctuation, actual demand, rapid technology change, delays or failures of customers’ tape-outs into wafer production, our ability to negotiate, monitor and enforce agreements for the determination and payment of royalties, any bug or fault in our technology which leads to significant damage to our technology and reputation, actual or potential litigation, semiconductor industry cycle and general economic conditions. Except as required by law, eMemory undertakes no obligation to update or revise any forward-looking statements, whether as a result of new information, future events, or otherwise.
Outline

• Business Model

• Review of Operations

• Growth Opportunity and Future Outlook

• Q & A
Nonvolatile Memory Classifications

- **Standalone NAND Flash with MLC+ECC**
- **Standalone NOR Flash**
- **Embedded Flash**
  - OTP (General MCU, Speech IC)
  - MTP
- **Embedded NAND Flash with MLC+ECC**
- **Standalone NOR Flash**
- **Embedded Flash**
- **EEPROM**

- **Embedded Flash replacement for program codes update infrequently**
- **EEPROM replacement for data update frequently**
SOC Block Diagram

Embedded Non Volatile Memory

Source: tsmc
## Embedded NVM Technologies

<table>
<thead>
<tr>
<th></th>
<th>ROM</th>
<th>eFuse (OTP)</th>
<th>Antifuse (OTP)</th>
<th>CMOS Floating Gate (OTP)</th>
<th>CMOS Floating Gate (MTP)</th>
<th>Embedded Flash</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Cell Structure</strong></td>
<td>Transistor</td>
<td>Poly Fuse</td>
<td>Antifuse</td>
<td>Floating Gate</td>
<td>Floating Gate</td>
<td>Floating Gate</td>
</tr>
<tr>
<td><strong>Standard CMOS Compatible</strong></td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td><strong>Bitcell Area</strong></td>
<td>&lt; 1</td>
<td>50</td>
<td>1</td>
<td>2</td>
<td>4</td>
<td>1</td>
</tr>
<tr>
<td><strong>Endurance</strong></td>
<td>No</td>
<td>No</td>
<td>&lt; 10</td>
<td>&lt; 10</td>
<td>10K-100K</td>
<td>100-1000K</td>
</tr>
<tr>
<td><strong>Density</strong></td>
<td>4Kb-1Mb</td>
<td>256bit-4Kb</td>
<td>16bit-1Mb</td>
<td>16Kb-1Mb</td>
<td>1Kb-2M</td>
<td>64Kb-4Mb</td>
</tr>
<tr>
<td><strong>Security</strong></td>
<td>Low</td>
<td>Low</td>
<td>High</td>
<td>High</td>
<td>High</td>
<td>High</td>
</tr>
<tr>
<td><strong>Additional Steps</strong></td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>+10 Mask</td>
</tr>
</tbody>
</table>

- ROM not programmable, eFuse cannot scale beyond 16Kb, embedded flash expensive and cannot scale after 40 nm
- eMemory’s IPs: OTP (antifuse, floating gate) and MTP (floating gate)
Considerations for IP Adoption

Generally, IP size is less than 10% of product size.

Customers Request
1. 100% IP Reliability
2. No Mask Adder
3. Low Testing Cost
4. On call Service
5. Acceptable IP Size
Inside Nonvolatile Memory IP

Where data is stored. Each cross point has a memory cell.

Program, Erase and Read operation control

Power supply for operations

X-Decoder & Control Circuit

Power

Y-Path

Memory Cell Array

Data input & output

Where data is stored. Each cross point has a memory cell.

Power supply for operations

X-Decoder & Control Circuit

Power

Y-Path

Memory Cell Array

Data input & output

Where data is stored. Each cross point has a memory cell.

Power supply for operations

X-Decoder & Control Circuit

Power

Y-Path

Memory Cell Array

Data input & output

Where data is stored. Each cross point has a memory cell.

Power supply for operations

X-Decoder & Control Circuit

Power

Y-Path

Memory Cell Array

Data input & output

Where data is stored. Each cross point has a memory cell.

Power supply for operations

X-Decoder & Control Circuit

Power

Y-Path

Memory Cell Array

Data input & output

Where data is stored. Each cross point has a memory cell.

Power supply for operations

X-Decoder & Control Circuit

Power

Y-Path

Memory Cell Array

Data input & output

Where data is stored. Each cross point has a memory cell.

Power supply for operations

X-Decoder & Control Circuit

Power

Y-Path

Memory Cell Array

Data input & output

Where data is stored. Each cross point has a memory cell.

Power supply for operations

X-Decoder & Control Circuit

Power

Y-Path

Memory Cell Array

Data input & output

Where data is stored. Each cross point has a memory cell.

Power supply for operations

X-Decoder & Control Circuit

Power

Y-Path

Memory Cell Array

Data input & output

Where data is stored. Each cross point has a memory cell.

Power supply for operations

X-Decoder & Control Circuit

Power

Y-Path

Memory Cell Array

Data input & output

Where data is stored. Each cross point has a memory cell.

Power supply for operations

X-Decoder & Control Circuit

Power

Y-Path

Memory Cell Array

Data input & output

Where data is stored. Each cross point has a memory cell.

Power supply for operations

X-Decoder & Control Circuit

Power

Y-Path

Memory Cell Array

Data input & output

Where data is stored. Each cross point has a memory cell.

Power supply for operations

X-Decoder & Control Circuit

Power

Y-Path

Memory Cell Array

Data input & output

Where data is stored. Each cross point has a memory cell.

Power supply for operations

X-Decoder & Control Circuit

Power

Y-Path

Memory Cell Array

Data input & output

Where data is stored. Each cross point has a memory cell.

Power supply for operations

X-Decoder & Control Circuit

Power

Y-Path

Memory Cell Array

Data input & output

Where data is stored. Each cross point has a memory cell.

Power supply for operations

X-Decoder & Control Circuit

Power

Y-Path

Memory Cell Array

Data input & output

Where data is stored. Each cross point has a memory cell.

Power supply for operations

X-Decoder & Control Circuit

Power

Y-Path

Memory Cell Array

Data input & output

Where data is stored. Each cross point has a memory cell.

Power supply for operations

X-Decoder & Control Circuit

Power

Y-Path

Memory Cell Array

Data input & output

Where data is stored. Each cross point has a memory cell.

Power supply for operations

X-Decoder & Control Circuit

Power

Y-Path

Memory Cell Array

Data input & output

Where data is stored. Each cross point has a memory cell.

Power supply for operations

X-Decoder & Control Circuit

Power

Y-Path

Memory Cell Array

Data input & output

Where data is stored. Each cross point has a memory cell.

Power supply for operations

X-Decoder & Control Circuit

Power

Y-Path

Memory Cell Array

Data input & output

Where data is stored. Each cross point has a memory cell.

Power supply for operations

X-Decoder & Control Circuit

Power

Y-Path

Memory Cell Array

Data input & output

Where data is stored. Each cross point has a memory cell.

Power supply for operations

X-Decoder & Control Circuit

Power

Y-Path

Memory Cell Array

Data input & output

Where data is stored. Each cross point has a memory cell.

Power supply for operations

X-Decoder & Control Circuit

Power

Y-Path

Memory Cell Array

Data input & output

Where data is stored. Each cross point has a memory cell.

Power supply for operations

X-Decoder & Control Circuit

Power

Y-Path

Memory Cell Array

Data input & output

Where data is stored. Each cross point has a memory cell.

Power supply for operations

X-Decoder & Control Circuit

Power

Y-Path

Memory Cell Array

Data input & output

Where data is stored. Each cross point has a memory cell.

Power supply for operations

X-Decoder & Control Circuit

Power

Y-Path

Memory Cell Array

Data input & output

Where data is stored. Each cross point has a memory cell.

Power supply for operations

X-Decoder & Control Circuit

Power

Y-Path

Memory Cell Array

Data input & output

Where data is stored. Each cross point has a memory cell.

Power supply for operations

X-Decoder & Control Circuit

Power

Y-Path

Memory Cell Array

Data input & output

Where data is stored. Each cross point has a memory cell.

Power supply for operations

X-Decoder & Control Circuit

Power

Y-Path

Memory Cell Array

Data input & output

Where data is stored. Each cross point has a memory cell.

Power supply for operations

X-Decoder & Control Circuit

Power

Y-Path

Memory Cell Array

Data input & output

Where data is stored. Each cross point has a memory cell.

Power supply for operations

X-Decoder & Control Circuit

Power

Y-Path

Memory Cell Array

Data input & output

Where data is stored. Each cross point has a memory cell.

Power supply for operations

X-Decoder & Control Circuit

Power

Y-Path

Memory Cell Array

Data input & output

Where data is stored. Each cross point has a memory cell.
About eMemory

• Largest Logic Non-Volatile Memory (NVM) IP company
• 234 employees (161 R&D)*.
• No fundraising from capital markets or bank loans since IPO in 2011.
• Over 90% of earnings distributed in cash dividends.

Note*: As of June 30th, 2017
Business Model

• Growth Metrics
  › No. of Embedded Platforms
  › No. of Design Licenses
  › Royalty

Upfront License Fee
(Technology & Design License)

1-2 years eMemory & foundry development
Technology License Revenue

1-2 years Fabless product development
Design License Revenue

3+ years Multiple applications & sales
Royalty Revenue Continues

Royalties
Collected directly from foundries upon volume production of customers’ chips
Worldwide Customers

<table>
<thead>
<tr>
<th></th>
<th>Taiwan</th>
<th>China</th>
<th>Korea</th>
<th>Japan</th>
<th>North America</th>
<th>Europe</th>
<th>Others</th>
</tr>
</thead>
<tbody>
<tr>
<td>Foundry</td>
<td>5</td>
<td>8</td>
<td>3</td>
<td>4</td>
<td>1</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>IDM</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>8</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Fabless</td>
<td>261</td>
<td>513</td>
<td>71</td>
<td>52</td>
<td>242</td>
<td>111</td>
<td>53</td>
</tr>
</tbody>
</table>

Embedded Wisely, Embedded Widely
## Patent Portfolio

<table>
<thead>
<tr>
<th></th>
<th>1Q 17</th>
<th>2Q 17</th>
<th>Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pending</td>
<td>244</td>
<td>232</td>
<td>- 12</td>
</tr>
<tr>
<td>Issued</td>
<td>416</td>
<td>453</td>
<td>+ 37</td>
</tr>
<tr>
<td>Total</td>
<td>660</td>
<td>685</td>
<td>+ 25</td>
</tr>
</tbody>
</table>

Note: As of June 30th, 2017
Quarterly Revenue Pattern

- 1st month: Receive **License Fees** of the month and **Royalty** from most foundries on previous quarter’s wafer shipments
- 2nd month: Receive **License Fees** of the month and **Royalty** from other foundries
- 3rd month: **License Fees** Only.

<table>
<thead>
<tr>
<th>Time Period</th>
<th>License Fees</th>
<th>Royalty</th>
</tr>
</thead>
<tbody>
<tr>
<td>1st month</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2nd month</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3rd month</td>
<td>License Fees Only</td>
<td></td>
</tr>
</tbody>
</table>

Thousands of NT dollars

![Bar Chart of Quarterly Revenue Pattern](chart.png)
Outline

• Business Model

• Review of Operations

• Growth Opportunity and Future Outlook

• Q & A
## Q2 Revenue Breakdown

### Thousands of NT dollars

<table>
<thead>
<tr>
<th></th>
<th>Q2 2017</th>
<th>Q1 2017</th>
<th>QoQ</th>
<th>Q2 2016</th>
<th>YoY</th>
<th>H1 2017</th>
<th>H1 2016</th>
<th>YoY</th>
</tr>
</thead>
<tbody>
<tr>
<td>Licensing</td>
<td>134,140</td>
<td>74,146</td>
<td>80.91%</td>
<td>77,715</td>
<td>72.61%</td>
<td>208,286</td>
<td>163,691</td>
<td>27.24%</td>
</tr>
<tr>
<td>Royalty</td>
<td>198,080</td>
<td>263,103</td>
<td>-24.71%</td>
<td>202,304</td>
<td>-2.09%</td>
<td>461,183</td>
<td>436,174</td>
<td>5.73%</td>
</tr>
<tr>
<td>Total</td>
<td>332,220</td>
<td>337,249</td>
<td>-1.49%</td>
<td>280,019</td>
<td>18.64%</td>
<td>669,469</td>
<td>599,865</td>
<td>11.60%</td>
</tr>
</tbody>
</table>

### Number of Licenses

<table>
<thead>
<tr>
<th></th>
<th>Q2 2017</th>
<th>Q1 2017</th>
<th>2016</th>
<th>2015</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology Licenses</td>
<td>8</td>
<td>5</td>
<td>43</td>
<td>28</td>
</tr>
<tr>
<td>Design Licenses</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NRE</td>
<td>13</td>
<td>8</td>
<td>56</td>
<td>57</td>
</tr>
<tr>
<td>Usage</td>
<td>79</td>
<td>88</td>
<td>311</td>
<td>349</td>
</tr>
</tbody>
</table>
## Financial Income Statement

Amount in Thousands of NT Dollars, except margins/EPS/ROE

<table>
<thead>
<tr>
<th></th>
<th>Q2 2017</th>
<th>Q1 2017</th>
<th>Q2 2016</th>
<th>change (QoQ)</th>
<th>change (YoY)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Revenue</strong></td>
<td>332,220</td>
<td>337,249</td>
<td>280,019</td>
<td>-1.5%</td>
<td>18.6%</td>
</tr>
<tr>
<td><strong>Gross Margin</strong></td>
<td>100%</td>
<td>100%</td>
<td>100%</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td><strong>Operating Expenses</strong></td>
<td>188,562</td>
<td>193,603</td>
<td>163,276</td>
<td>-2.6%</td>
<td>15.5%</td>
</tr>
<tr>
<td><strong>Operating Margin</strong></td>
<td>43.2%</td>
<td>42.6%</td>
<td>41.7%</td>
<td>0.6ppts</td>
<td>1.5ppts</td>
</tr>
<tr>
<td><strong>Net Income</strong></td>
<td>135,610</td>
<td>151,378</td>
<td>106,245</td>
<td>-10.4%</td>
<td>27.6%</td>
</tr>
<tr>
<td><strong>Net Margin</strong></td>
<td>40.8%</td>
<td>44.9%</td>
<td>37.9%</td>
<td>-4.1ppts</td>
<td>2.9ppts</td>
</tr>
<tr>
<td><strong>EPS</strong></td>
<td>1.79</td>
<td>2.00</td>
<td>1.40</td>
<td>-10.5%</td>
<td>27.9%</td>
</tr>
<tr>
<td><strong>ROE</strong></td>
<td>29.6%</td>
<td>30.2%</td>
<td>24.5%</td>
<td>-0.6ppts</td>
<td>5.1ppts</td>
</tr>
</tbody>
</table>

Note: Revenue amount in US dollars, QoQ growth of 2.2% and YoY growth of 26.8%.
Technology Licensing

Number of Licenses

<table>
<thead>
<tr>
<th>Year</th>
<th>2014</th>
<th>2015</th>
<th>2016</th>
<th>H1 2017</th>
</tr>
</thead>
<tbody>
<tr>
<td>License</td>
<td>21</td>
<td>28</td>
<td>43</td>
<td>13</td>
</tr>
</tbody>
</table>

Note: Terms (including number of process platforms and licensing fees) for each technology license are set contractually. Payments are made according to set milestones, and there are no particular seasonal factors involved.
New Technologies Under Development

• New technologies being developed for 104 platforms by Q2 17.

• 21 for NeoBit, 40 for NeoFuse, 20 for NeoEE, and 23 for NeoMTP.

<table>
<thead>
<tr>
<th>Platform</th>
<th>7/10nm</th>
<th>12/14/16nm</th>
<th>28nm</th>
<th>40nm</th>
<th>55/65nm</th>
<th>80/90nm</th>
<th>0.11~0.13um</th>
<th>0.15~0.18um</th>
<th>&gt;0.25um</th>
</tr>
</thead>
<tbody>
<tr>
<td>NeoBit</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>8</td>
<td>13</td>
<td>-</td>
</tr>
<tr>
<td>NeoFuse</td>
<td>3</td>
<td>3</td>
<td>8</td>
<td>3</td>
<td>10</td>
<td>6</td>
<td>4</td>
<td>3</td>
<td>-</td>
</tr>
<tr>
<td>NeoEE</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>3</td>
<td>17</td>
<td>-</td>
</tr>
<tr>
<td>NeoMTP</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>1</td>
<td>2</td>
<td>-</td>
<td>7</td>
<td>13</td>
<td>-</td>
</tr>
</tbody>
</table>

Note: As for June 30th, 2017
## Technology Developments by Processes

### 12" Fabs

<table>
<thead>
<tr>
<th>NVM Type</th>
<th>Process Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>OTP</td>
<td>FF</td>
</tr>
<tr>
<td>OTP, MTP</td>
<td>HV-DDI, LP, eFlash</td>
</tr>
<tr>
<td>OTP, MTP</td>
<td>LP, HV-DDI, HV-OLED, DRAM, CIS, eFlash</td>
</tr>
<tr>
<td>OTP, MTP</td>
<td>HV-DDI, HV-OLED, LP, eFlash</td>
</tr>
<tr>
<td>OTP</td>
<td>HV-DDI, BCD, Generic</td>
</tr>
<tr>
<td>OTP</td>
<td>BCD</td>
</tr>
</tbody>
</table>

### 8" Fabs

<table>
<thead>
<tr>
<th>NVM Type</th>
<th>Process Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>OTP</td>
<td>HV-DDI, LL</td>
</tr>
<tr>
<td>OTP, MTP</td>
<td>HV-DDI, BCD, LP, RF, CIS, LL, Green</td>
</tr>
<tr>
<td>OTP, MTP</td>
<td>Generic, LP, LL, MR, HV, Green, BCD</td>
</tr>
<tr>
<td>OTP</td>
<td>BCD</td>
</tr>
<tr>
<td>OTP</td>
<td>UHV</td>
</tr>
</tbody>
</table>

*Note: As of June 30th, 2017*
Design Licensing (New Tape-Out)

- A total 188 NTO in H1 2017 (367@2016, 406@2015, 445@2014, 393@2013)

Note*: As the applications of MCU at several foundries have gradually entered mass production, and the business model of the main foundry partner which provides green process has shifted to — eMemory licenses IP cell to the foundry for it to provide direct design service to customers — as the result, the new tape out number of MCU has been affected, but the royalty coming from IP cell usage continues to roll in.

In summary, even the new tape out number of MCU is lower than before; the corresponding wafer output and royalty continue to grow.

Embedded Wisely, Embedded Widely
Cumulative Licenses Drive Future Royalties

Cumulative design licenses > 3,710

- No. of New Design Licenses in the Corresponding Period
- No. of Cumulative Design Licenses
- Royalty

Note 1: Due to the 2009 recession, royalty income was down 1.5% from the previous year.
Note 2: Prepaid royalty from a single customer contributed to 2010 annual growth of 67%, followed by a drop of 6.3% in 2011.
Note 3: CAGR for 2009-2013 was 30%.
eMemory IP’s Penetration Rates in T Company (in US$revenue)

<table>
<thead>
<tr>
<th>Process node</th>
<th>*% of T</th>
<th>Q2 17</th>
<th>Q1 17</th>
<th>2016</th>
<th>2015</th>
</tr>
</thead>
<tbody>
<tr>
<td>8” 0.25/0.35</td>
<td>3%</td>
<td>44.84%</td>
<td>37.05%</td>
<td>28.15%</td>
<td>33.49%</td>
</tr>
<tr>
<td>0.15/0.16/0.18</td>
<td>11%</td>
<td>7.36%</td>
<td>9.10%</td>
<td>12.43%</td>
<td>8.73%</td>
</tr>
<tr>
<td>0.11/0.13</td>
<td>3%</td>
<td>58.76%</td>
<td>41.92%</td>
<td>42.61%</td>
<td>29%</td>
</tr>
<tr>
<td>12” 80/90nm</td>
<td>5%</td>
<td>12.73%</td>
<td>10.96%</td>
<td>12.50%</td>
<td>19.85%</td>
</tr>
<tr>
<td>55/65nm</td>
<td>10%</td>
<td>4.73%</td>
<td>3.50%</td>
<td>3.59%</td>
<td>0.55%</td>
</tr>
<tr>
<td>40/45nm</td>
<td>13%</td>
<td>0%</td>
<td>0%</td>
<td>0%</td>
<td>0%</td>
</tr>
<tr>
<td>28nm</td>
<td>27%</td>
<td>0.18%</td>
<td>0.56%</td>
<td>0.55%</td>
<td>0.05%</td>
</tr>
<tr>
<td>16/20nm</td>
<td>26%</td>
<td>0%</td>
<td>0%</td>
<td>0%</td>
<td>0%</td>
</tr>
<tr>
<td>8” 8”</td>
<td>18%</td>
<td>21.77%</td>
<td>16.13%</td>
<td>18.86%</td>
<td>16.64%</td>
</tr>
<tr>
<td>12” 12”</td>
<td>82%</td>
<td>1.43%</td>
<td>1.15%</td>
<td>1.44%</td>
<td>1.87%</td>
</tr>
<tr>
<td>Total</td>
<td>100%</td>
<td>5.07%</td>
<td>3.54%</td>
<td>4.27%</td>
<td>4.76%</td>
</tr>
</tbody>
</table>

* T company’s Q2 2017 revenues broken down by process nodes
Outline

• Business Model
• Review of Operations
• Growth Opportunity and Future Outlook
• Q & A
eMemory’s NVM Technologies

• Logic NVM portfolio offers one-stop-shop solution.
  › Compatible to any process
  › Robust structure
  › Low process cost
  › Competitive macro sizes
  › Easy integration
  › Easy porting

<table>
<thead>
<tr>
<th>eMemory’s NVM Technology</th>
<th>OTP</th>
<th>MTP</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>NeoBit</td>
<td>NeoFuse</td>
</tr>
<tr>
<td>Product Type</td>
<td>OTP</td>
<td>OTP</td>
</tr>
<tr>
<td>Endurance (Cycles)</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>Additional Mask Steps</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Technology</td>
<td>Floating gate</td>
<td>Anti-Fuse</td>
</tr>
<tr>
<td>Scalability</td>
<td>Simple</td>
<td>Simple</td>
</tr>
<tr>
<td>Memory Density</td>
<td>HD &lt; 512Kb</td>
<td>&lt; 4Mb</td>
</tr>
</tbody>
</table>
Applications by Technology

<table>
<thead>
<tr>
<th>12&quot;</th>
<th>8&quot;</th>
</tr>
</thead>
<tbody>
<tr>
<td>7nm</td>
<td>10nm</td>
</tr>
</tbody>
</table>

NeoBit

NeoFuse

NeoFlash

NeoEE

NeoMTP

Embedded Wisely, Embedded Widely
Opportunity at all Price Points

- eMemory Inside today

Opportunity

$400-700
(0.5um-0.25um)

$750-1,000
(0.18um-0.11um)

$1,000-4,000
(90nm-55nm)

$4,000-8,000
(40nm-16nm)

Average Selling Price of Wafer

Note: 2.2 million 8” equivalent wafers with eMemory IP were shipped in 2013. (~5% of WW foundry shipment)
eMemory IP in Smart Phone

- Capacitive Touch Panel Controller
- LCD Driver
- Connector
- PMIC/PMU
- NFC
- Camera Module
- Fuel Gauge
- Battery
- Ambient Sensor
- Proximity Sensor
- Accel.-sensor
- Mag.-sensor
- Gyro-sensor
- Base Band
- Application Processor

Source: eMemory Marketing

Embedded Wisely, Embedded Widely
Benefits from Using eMemory IPs

**Design-in for**
1. Trimming
2. Parameter Setting
3. Code Storage
4. Identification Setting
5. Encryption
6. Function Selection

**IC Design**

**CP Test**

- CP level
  1. Trim: output voltage or current
  2. Parameter Setting: default value
  3. Code Storage: default F/W code

**Package/FT level**
1. Trim: SPEC shift
2. Parameter Setting: cross chip optimization
3. Identification Setting: manufacturer resume
4. Function Selection: setting for target market

**System Assembling**

1. Parameter Setting: cross chip optimization
2. Code Storage: F/W code modification
3. Identification Setting: manufacturer resume
4. Encryption: Security algorithm or key storage

Embedded Wisely, Embedded Widely
Invisibility for Security

• Provide “Invisible Hardware Key” for invisible storage
• Prevent reverse-engineering to detect content of security key
• Protect firmware and hardware of ICs from pirating
• Extend & protect customer’s business

eFuse Key: Data is easily observed

Invisible Hardware Key: Data is hard to be detected
Security & Protection

Authorized Product

Security IP/Code by Authorized Use

Fake Product

Can NOT Work w/o Security IP/Code

re-produce

reverse copy

without protection

with protection

Authorized Product

reverse copy

re-produce
OTP for security Key storage

Source: Rambus crypto manager platform
NeoPUF for Security Key Generation

Source: Rambus crypto manager platform
What is **Physical Unclonable Functions**

Collision Probability $\approx 1/15B \approx 1/2^{34}$  
Collision Probability $= 1/2^{\text{Bits Stream Length}}$
NeoPUF Technology

IC Design

eMemory IP

Design-in
Customized SPEC & Function are designed for customer demands

Manufacturing
Process Variation is introduced during manufacturing process (+0 mask logic process)

Wafer Process

CP / FT Test

Product Testing
Random Noise is enhanced and generated randomly

System Assembling

Random Seed activates Identification, Encryption, Authentication, Security Key Storage

Embedded Wisely, Embedded Widely
NeoPUF - Essential Security Component

• Unique & unclonable hardware root of trust
• Authentic random number generator
• Every chip equipped with its own “fingerprint”
• Multiple functions:
  › Encryption-decryption key to secure stored data
  › Public-Private key pair generation
  › Digital signature of hardware
  › Device secure booting
NeoPUF – Authentication & Security Everywhere

Smart Payment/IoT Device/Data Center

Data Storage Security

Hardware ID Tracking
Crossing the Chasm

Customers

Time

NeoMTP  NeoEE  NeoFuse  NeoBit

MRAM  NeoPUE
Security with eMemory IPs

Security for System Service

Cloud Processing

ID & Authentication
Data Integrity
Access Control

HW Protection
Invisible Key for
Anti-Cloning

Security Lock

HW-SW/FW Lock

HW Key

FW (OS) with
security key

Security IP/Code by
Authorized Use
NVM IP Demand in IoT

All Smart Systems

Basic Technology
- Sensing
  - Accelerometer
  - Magnetometer
  - Gyroscope
  - Pressure
  - Altimeter
  - Temperature

- Embedded Processing
  - MCU
  - MPU
  - Hybrid MCU/MPU
  - Network Processor

- Connectivity
  - NFC
  - GPS
  - BT/BTLE
  - Wi-Fi
  - Cellular
  - Sub-Gig
  - ZigBee
  - RFID

IC Types

NVM IP Function
- Encryption/Security
- Function Selection
- Trimming/Calibration
- F/W code storage
- Parameter Setting
- ID Setting

Embedded Wisely, Embedded Widely
Autotronics with eMemory IPs

Intelligent drive
Distronic system

Infotainment system

Sensor system

Auto parking system

Blind Spot Warning System
Cockpit System

OBU & GPS

Keyless door

Rear view system

Embedded Wisely, Embedded Widely
Outlook for Q3 and beyond

Revenue growth to accelerate in H2 2017

• Key drivers to licensing revenue:
  › Worldwide foundry partners keep developing advanced processes and MTP platforms.
  › We’re establishing partnerships with more foundries worldwide.
  › Our growing IP library will also boost design license revenue.

• Key drivers to royalty revenue:
  8-inch processes
  › Fingerprint royalty grow explosively due to an expansion from high-end to mid-low smartphones markets as well as our market share gains.
Outlook for Q3 and beyond

› PMIC royalty will increase strongly with content increase of new smartphones. Growths will be driven by the ramp of new products by a US smartphone maker in H2, as well as a shift of business terms with the largest US chipmaker from “one-time fee” to “royalty-based”.

› MTP IP series start contributing to royalty with more design-wins.

› Automotive applications start generating royalty.

12-inch processes

› With display technology migrating toward TDDI and OLED, our customers continue volume production of high-end TDDI (55nm) and OLED (40nm) products.

› STB, Multimedia and Network-related applications have been taped out subsequently in 28nm and below.
Outlook for Q3 and beyond

• R&D developments
  › Our IP has been taped out at 12nm and 22nm SOI process. The 7nm IP first taped out in April at one foundry, and one more tape-out expected in September at another foundry.
  › NeoPUF, our security IP, has been taped out at a major foundry and is to be designed into products by the end of this year.
  › Autotronic customers have started volume production beginning this year.
Key Growth Drivers

- **Growth in application per mobile devices**
  - More chip applications per smartphone/tablet product.

- **Growth into more markets**
  - From consumer electronics and mobile devices to wearable devices.
  - Adding new NVM product lines further enable more product applications.

- **Growth in advanced technology**
  - Higher royalty per wafer is contributed from more advanced technology nodes.

- **Great IoT era**
  - Embedded Logic NVM will be a must.
Q & A
Embedded Wisely, Embedded Widely