ememory

A Leading Logic NVM Company

IPR Notice

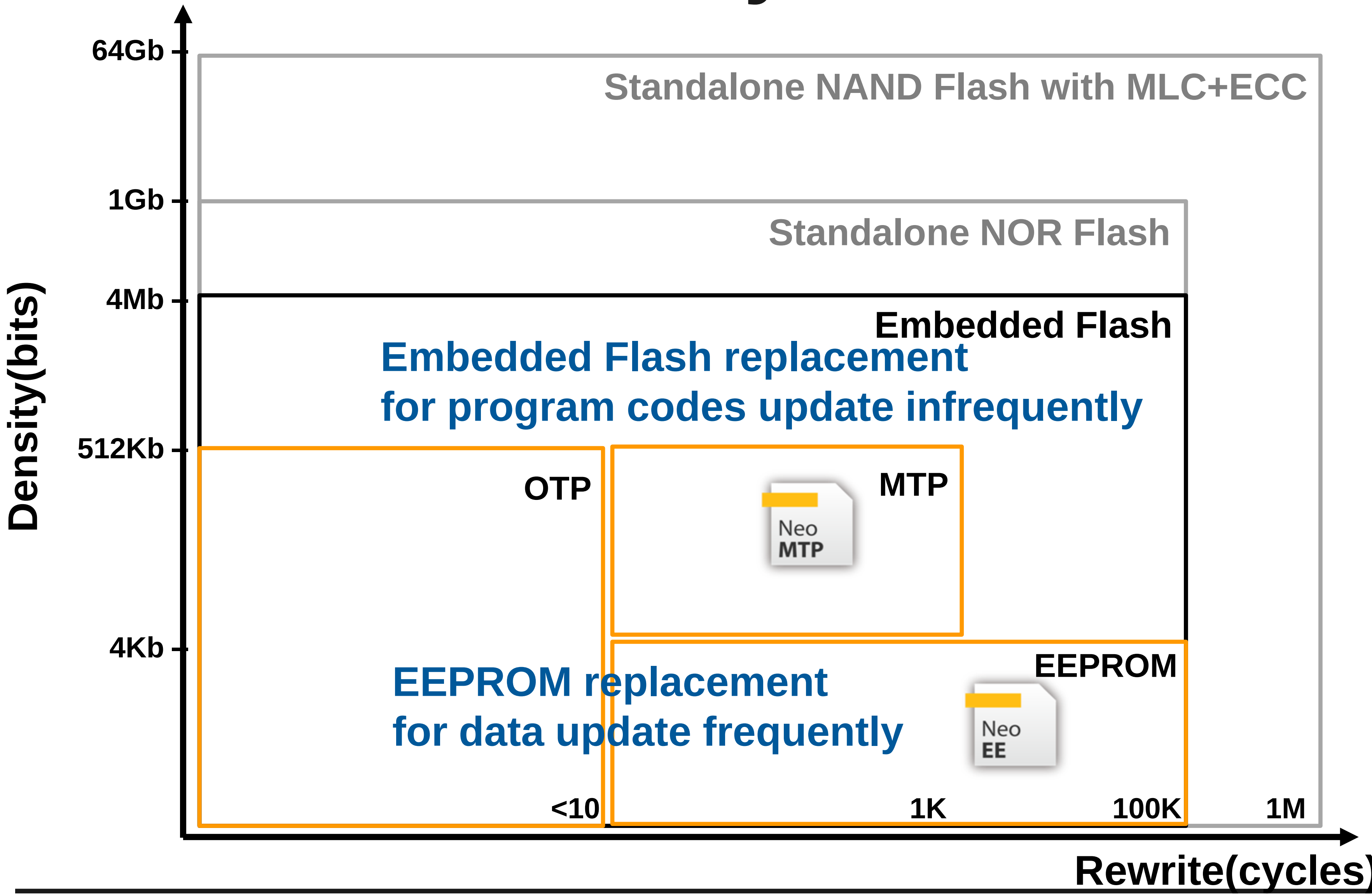
Cautionary Statement

This presentation contains forward-looking statements, which are subject to risk factors associated with semiconductor and intellectual property business. It is believed that the expectations reflected in these statements are reasonable. But they may be affected by a variety of variables, many of which are beyond our control. These variables could cause actual results or trends to differ materially which include, but are not limited to: wafer price fluctuation, actual demand, rapid technology change, delays or failures of customers' tape-outs into wafer production, our ability to negotiate, monitor and enforce agreements for the determination and payment of royalties, any bug or fault in our technology which leads to significant damage to our technology and reputation, actual or potential litigation, semiconductor industry cycle and general economic conditions. Except as required by law, eMemory undertakes no obligation to update or revise any forward-looking statements, whether as a result of new information, future events, or otherwise.

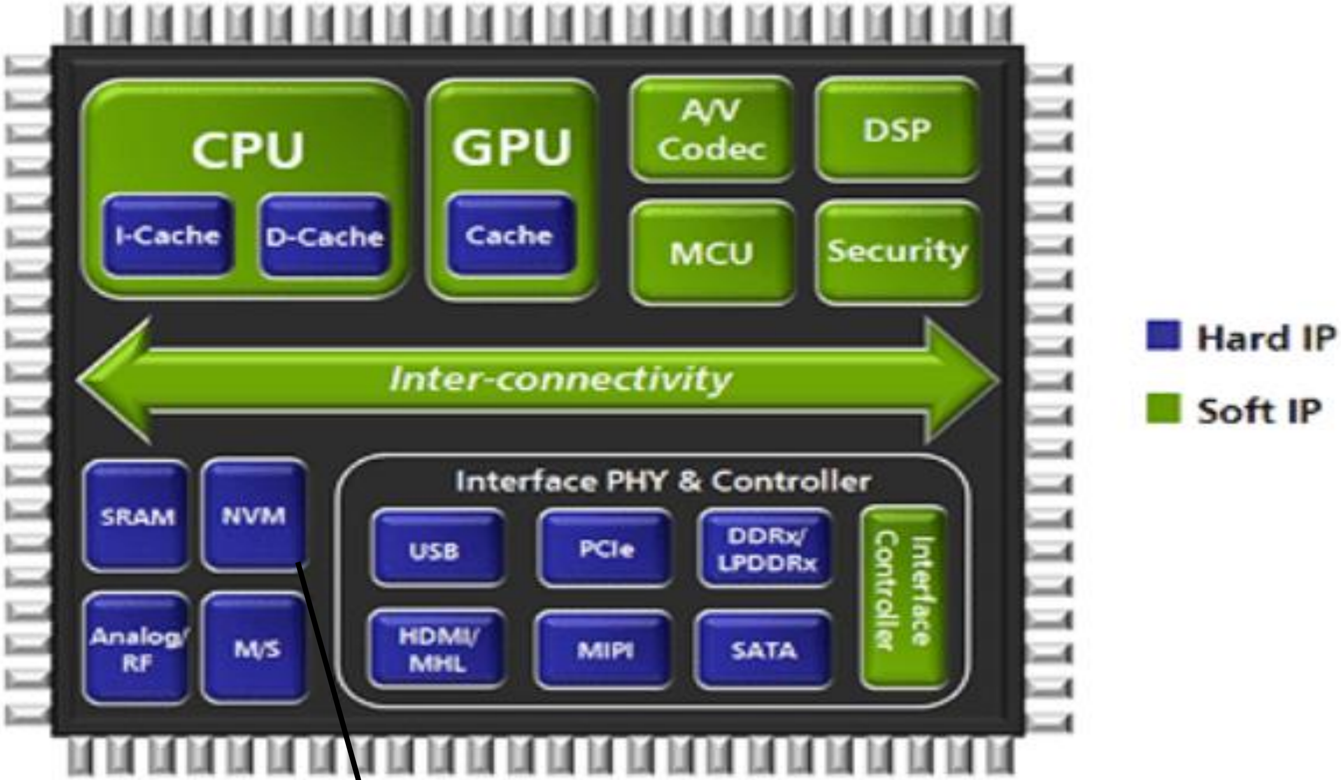
Outline

- Business Model
- Review of Operations
- Growth Opportunity and Future Outlook
- Q & A

Nonvolatile Memory Classifications



SOC Block Diagram



Embedded Non Volatile Memory

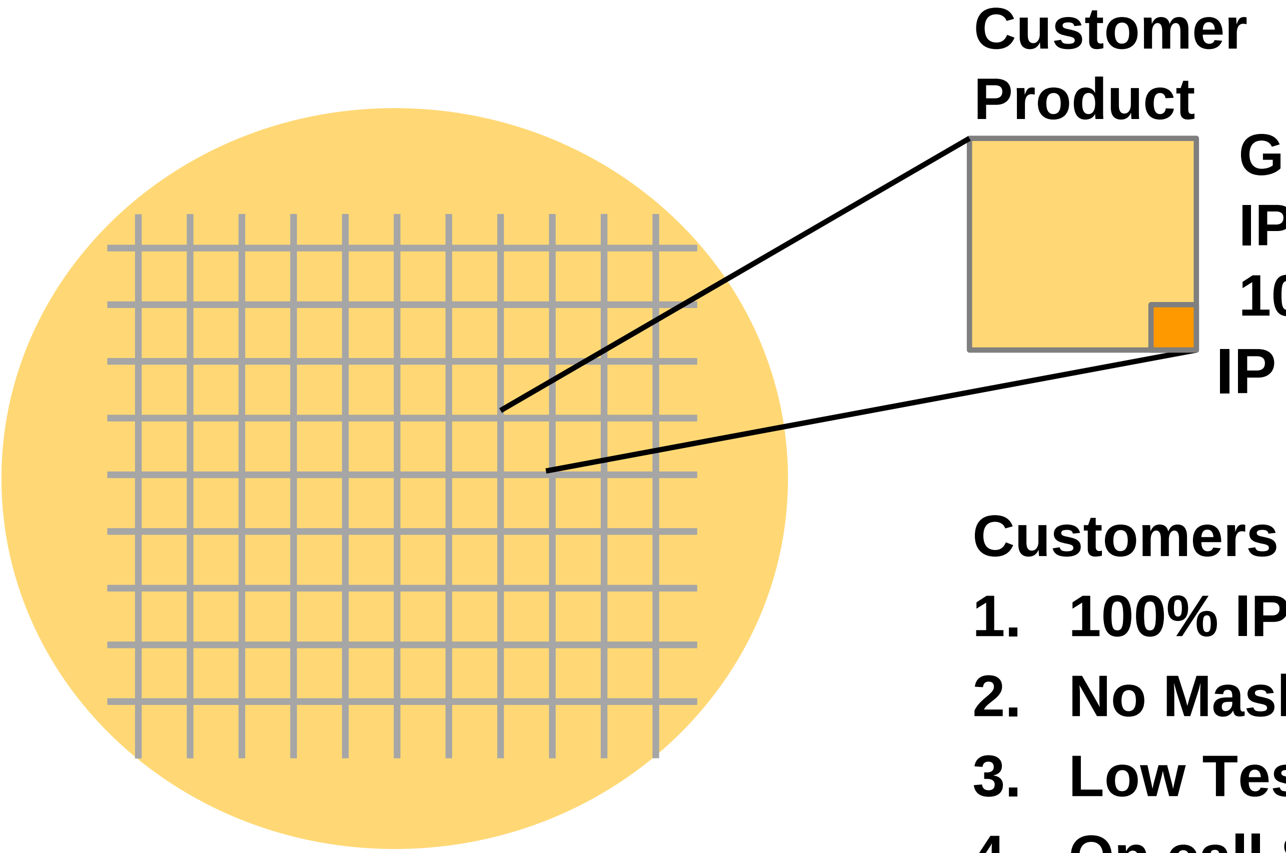
Source：tsmc

Embedded NVM Technologies

	ROM	eFuse (OTP)	Antifuse (OTP)	CMOS Floating Gate (OTP)	CMOS Floating Gate (MTP)	Embedded Flash
Cell Structure	Transistor	Poly Fuse	Antifuse	Floating Gate	Floating Gate	Floating Gate
Standard CMOS Compatible	Yes	Yes	Yes	Yes	Yes	No
Bitcell Area	< 1	50	1	2	4	1
Endurance	No	No	< 10	< 10	10K-100K	100-1000K
Density	4Kb-1Mb	256bit-4Kb	16bit-1Mb	16Kb-1Mb	1Kb-2M	64Kb-4Mb
Security	Low	Low	High	High	High	High
Additional Steps	None	None	None	None	None	+10 Mask

- **ROM not programmable, eFuse cannot scale beyond 16Kb, embedded flash expensive and cannot scale after 40 nm**
- **eMemory's IPs: OTP (antifuse, floating gate) and MTP (floating gate)**

Considerations for IP Adoption

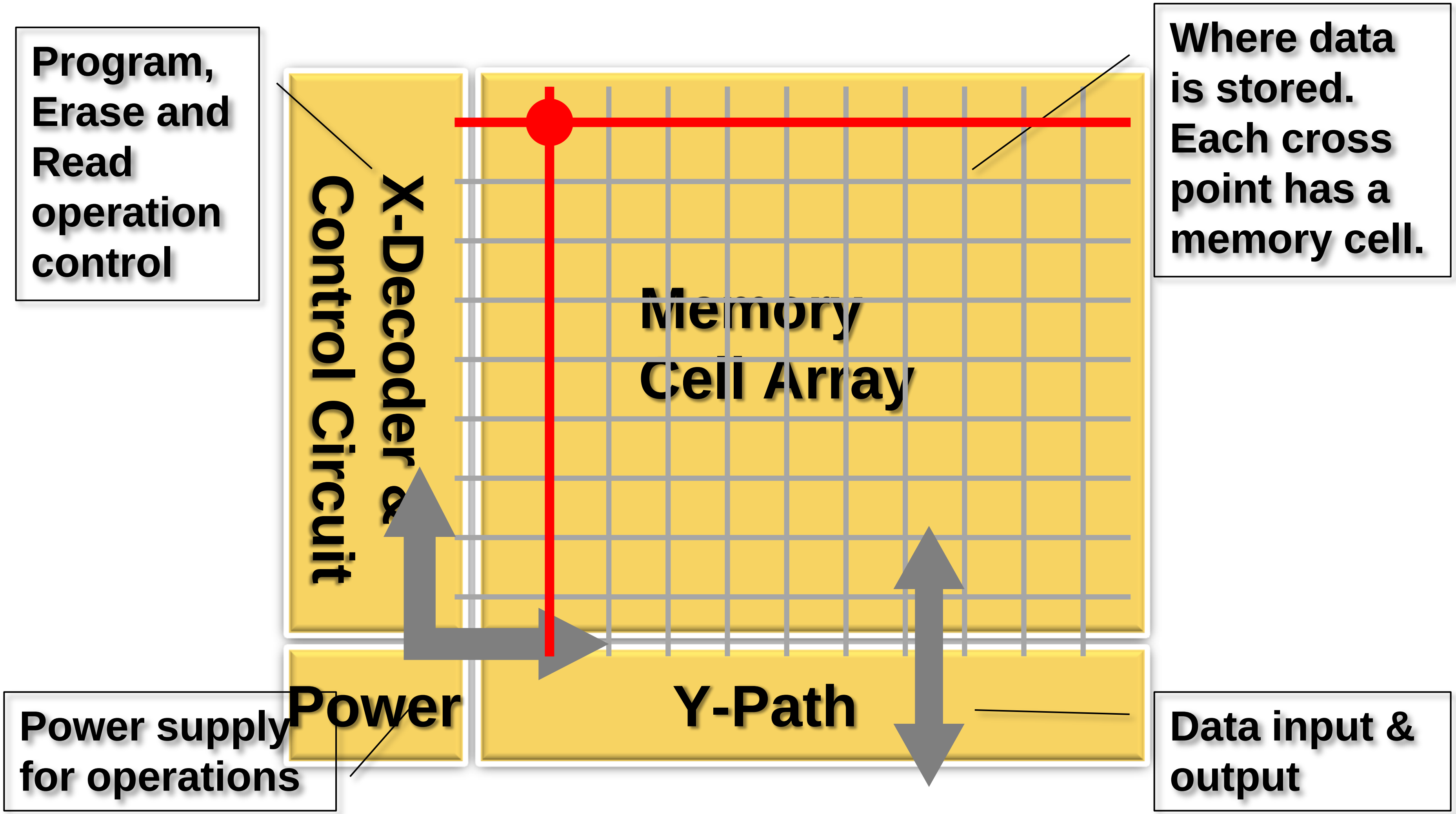


Generally, IP size is less than 10% of product size

Customers Request

1. **100% IP Reliability**
2. **No Mask Adder**
3. **Low Testing Cost**
4. **On call Service**
5. **Acceptable IP Size**

Inside Nonvolatile Memory IP



About eMemory

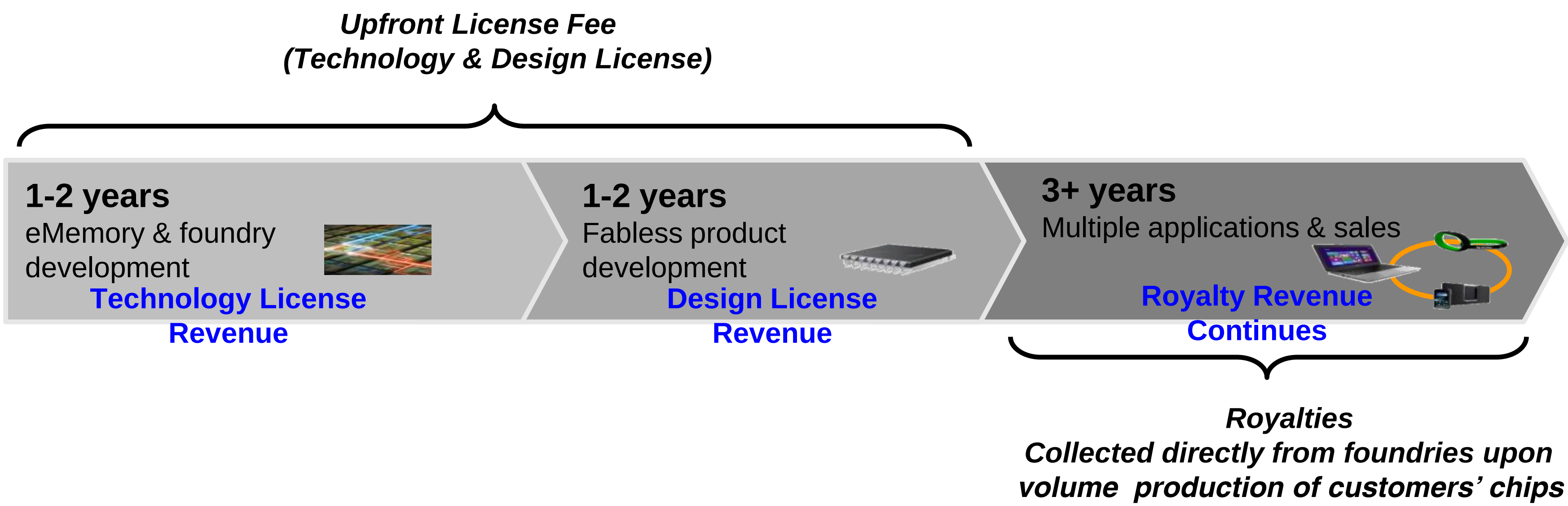
Founded 2000	First Customer 2002	Turned Profit 2005	IPO 2011

- **Largest Logic Non-Volatile Memory (NVM) IP company**
- **234 employees (161 R&D)*.**
- **No fundraising from capital markets or bank loans since IPO in 2011.**
- **Over 90% of earnings distributed in cash dividends.**

Note*: As of June 30th, 2017

Business Model

- **Growth Metrics**
  - **No. of Embedded Platforms**
  - **No. of Design Licenses**
  - **Royalty**



Worldwide Customers

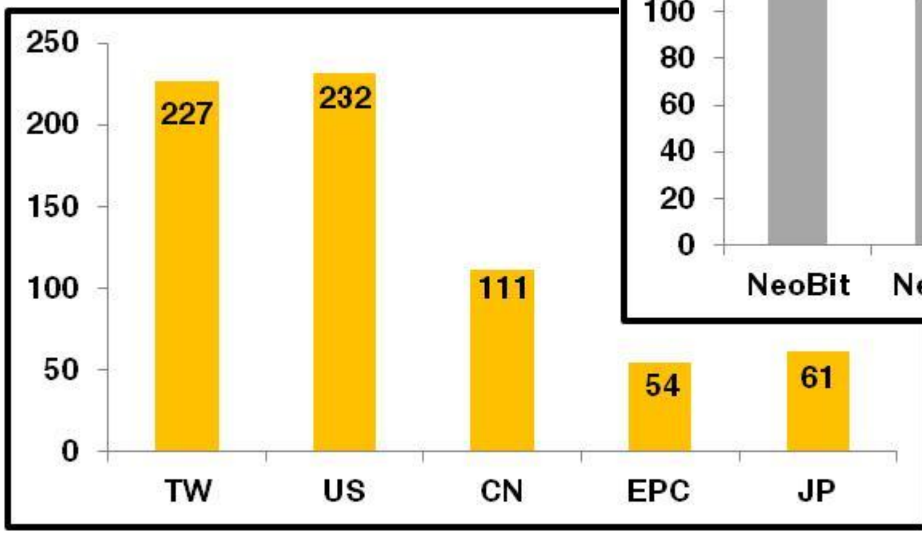
	Taiwan	China	Korea	Japan	North America	Europe	Others
Foundry	5	8	3	4	1	2	1
IDM	0	0	0	8	2	1	0
Fabless	261	513	71	52	242	111	53

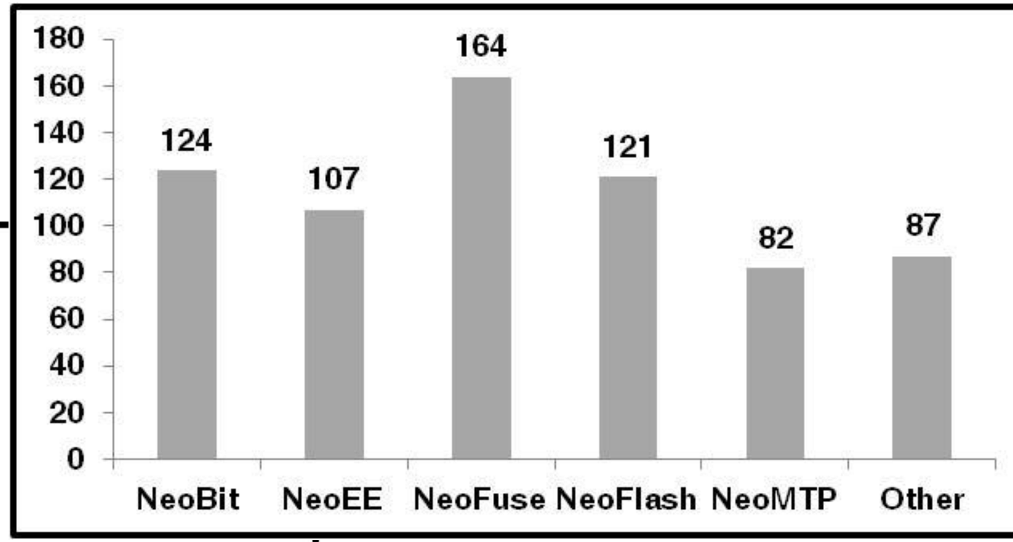
Foundry

IDM

Patent Portfolio

	1Q 17	2Q 17	Change
Pending	244	232	- 12
Issued	416	453	+ 37
Total	660	685	+ 25

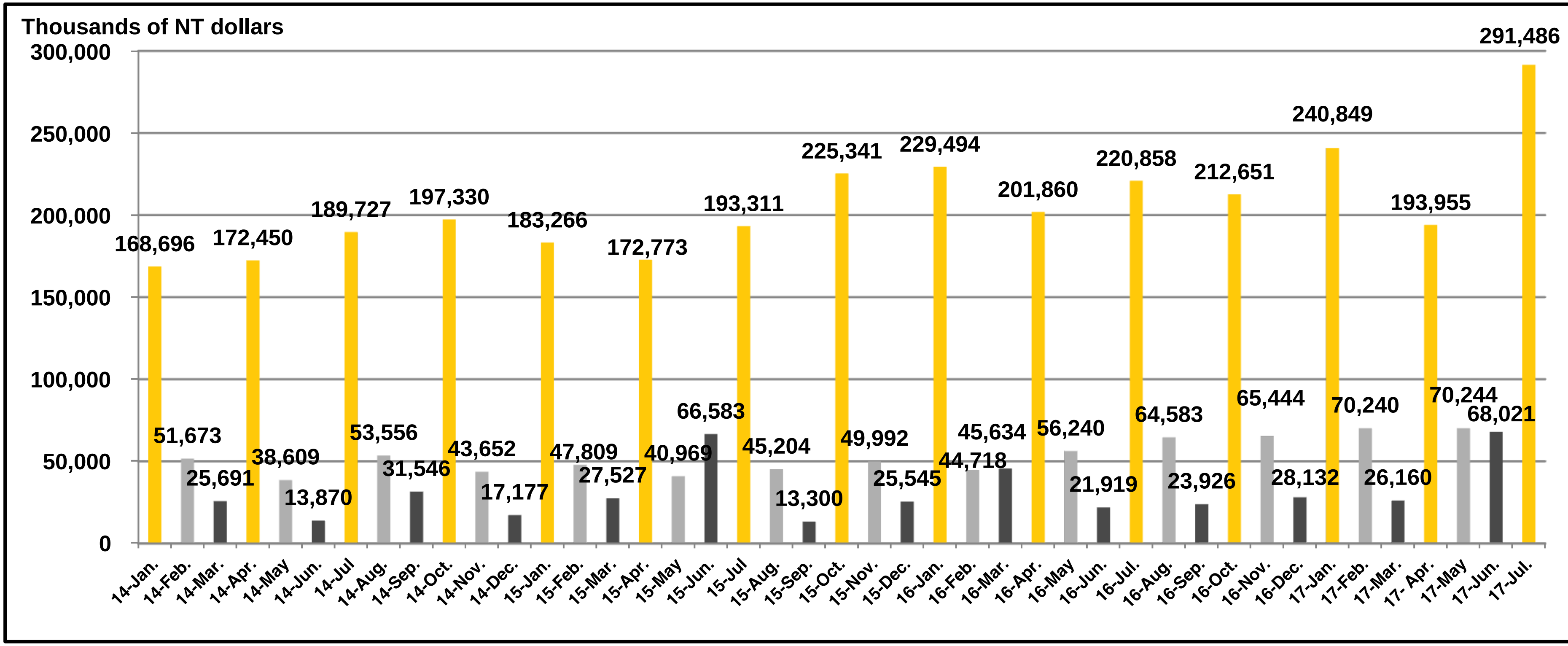




Note: As of June 30th, 2017

Quarterly Revenue Pattern

- 1st month: Receive **License Fees** of the month and **Royalty** from most foundries on previous quarter's wafer shipments
- 2nd month: Receive **License Fees** of the month and **Royalty** from other foundries
- 3rd month: **License Fees** Only.



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Q2 Revenue Breakdown

Thousands of NT dollars

	Q2 2017	Q1 2017	QoQ	Q2 2016	YoY	H1 2017	H1 2016	YoY
Licensing	134,140	74,146	80.91%	77,715	72.61%	208,286	163,691	27.24%
Royalty	198,080	263,103	-24.71%	202,304	-2.09%	461,183	436,174	5.73%
Total	332,220	337,249	-1.49%	280,019	18.64%	669,469	599,865	11.60%

Number of Licenses

		Q2 2017	Q1 2017	2016	2015
Technology Licenses		8	5	43	28
Design Licenses	NRE	13	8	56	57
	Usage	79	88	311	349

Financial Income Statement

Amount in Thousands of NT Dollars, except margins/EPS/ROE

	Q2 2017	Q1 2017	Q2 2016	change (QoQ)	change (YoY)
Revenue	332,220	337,249	280,019	-1.5%	18.6%
Gross Margin	100%	100%	100%	-	-
Operating Expenses	188,562	193,603	163,276	-2.6%	15.5%
Operating Margin	43.2%	42.6%	41.7%	0.6ppts	1.5ppts
Net Income	135,610	151,378	106,245	-10.4%	27.6%
Net Margin	40.8%	44.9%	37.9%	-4.1ppts	2.9ppts
EPS	1.79	2.00	1.40	-10.5%	27.9%
ROE	29.6%	30.2%	24.5%	-0.6ppts	5.1ppts

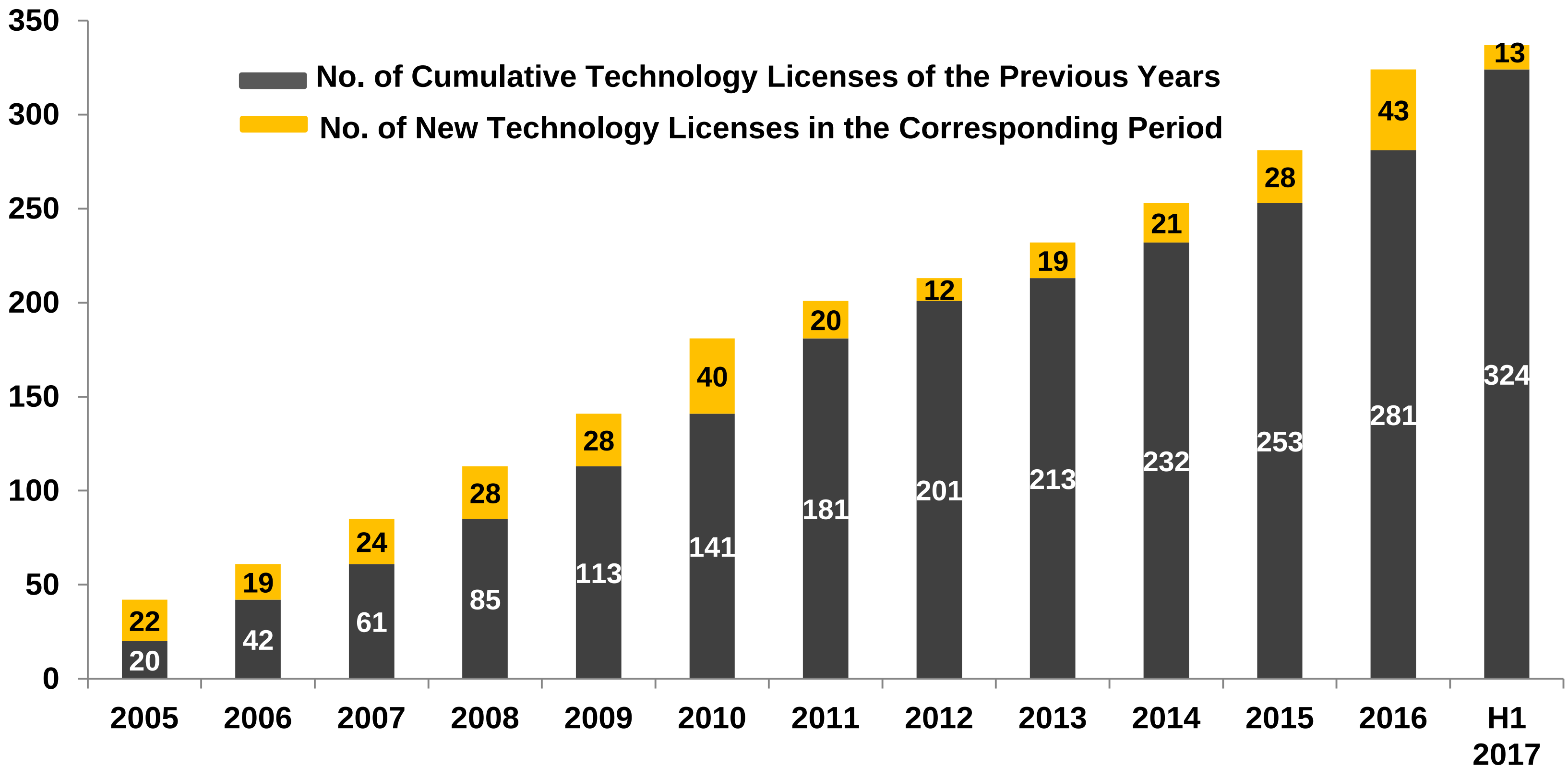
Note：Revenue amount in US dollars, QoQ growth of 2.2% and YoY growth of 26.8%.

Technology Licensing

Number of Licenses

Year	2014	2015	2016	H1 2017
License	21	28	43	13

Note: Terms (including number of process platforms and licensing fees) for each technology license are set contractually. Payments are made according to set milestones, and there are no particular seasonal factors involved.



New Technologies Under Development

- **New technologies being developed for 104 platforms by Q2 17.**
- **21 for NeoBit, 40 for NeoFuse, 20 for NeoEE, and 23 for NeoMTP.**

	7/10nm	12/14/16nm	28nm	40nm	55/65nm	80/90nm	0.11~ 0.13um	0.15~ 0.18um	>0.25 um
NeoBit	-	-	-	-	-	-	8	13	-
NeoFuse	3	3	8	3	10	6	4	3	-
NeoEE	-	-	-	-	-	-	3	17	-
NeoMTP	-	-	-	-	1	2	7	13	-

Note: As for June 30th, 2017

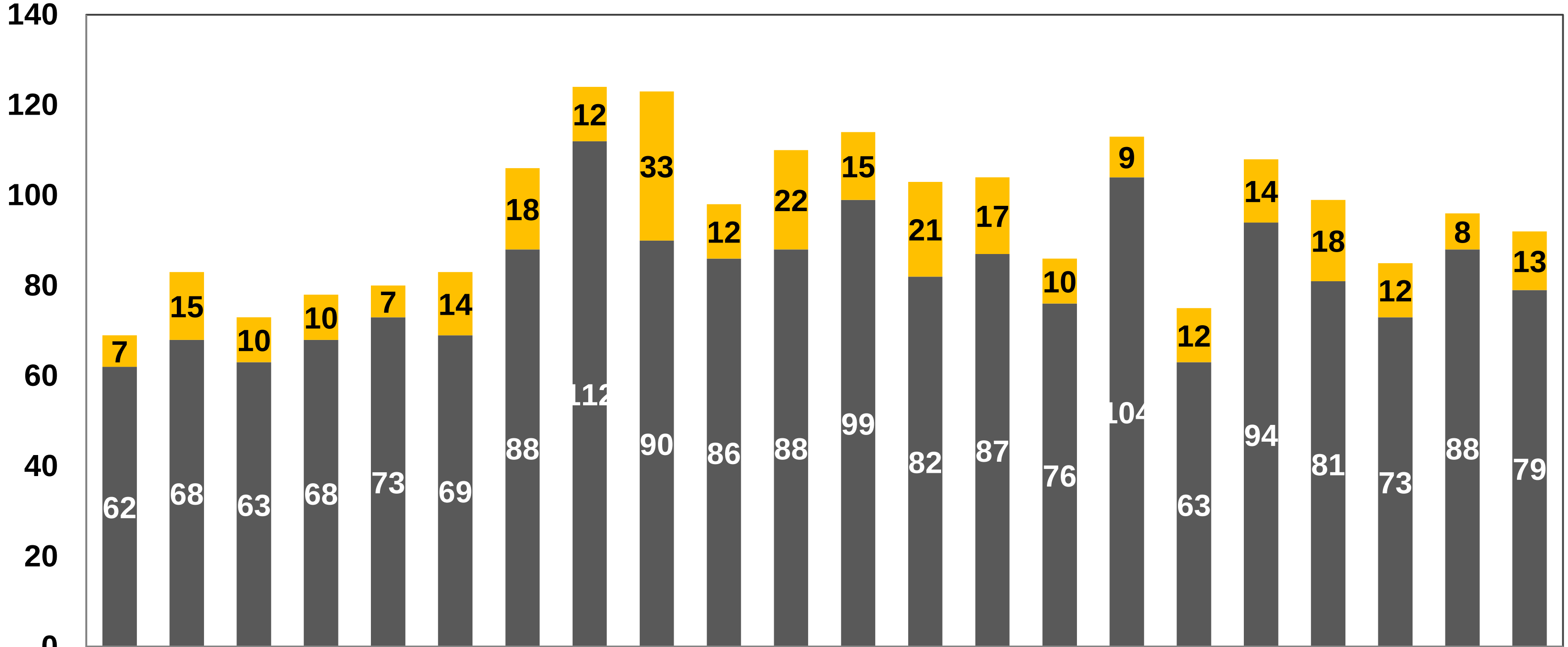
Technology Developments by Processes

12" Fabs	Production	Development	NVM Type	Process Type
7/10nm	0	3	OTP	FF
12/14/16nm	2	3	OTP	FF+
28nm	8	8	OTP	LP/HPM, HLP/HPM, LPS
40nm	8	3	OTP, MTP	HV-DDI, LP, eFlash
55/65nm	14	11	OTP, MTP	LP, HV-DDI, HV-OLED, DRAM, CIS, eFlash
80/90nm	6	5	OTP, MTP	HV-DDI, HV-OLED, LP, eFlash
0.13/0.11um	9	1	OTP	HV-DDI, BCD, Generic
0.18um	1	0	OTP	BCD
Total	48	34		

8" Fabs	Development	NVM Type	Process Type
90nm	3	OTP	HV-DDI, LL
0.13/0.11um	21	OTP, MTP	HV-DDI, BCD, LP, RF, CIS, LL, Green
0.18/0.16/0.152um	46	OTP, MTP	Generic, LP, LL, MR, HV, Green, BCD
0.25um	0	OTP, MTP	BCD
0.35um	0	OTP	UHV
Total	70		Note: As of June 30th, 2017

Design Licensing (New Tape-Out)

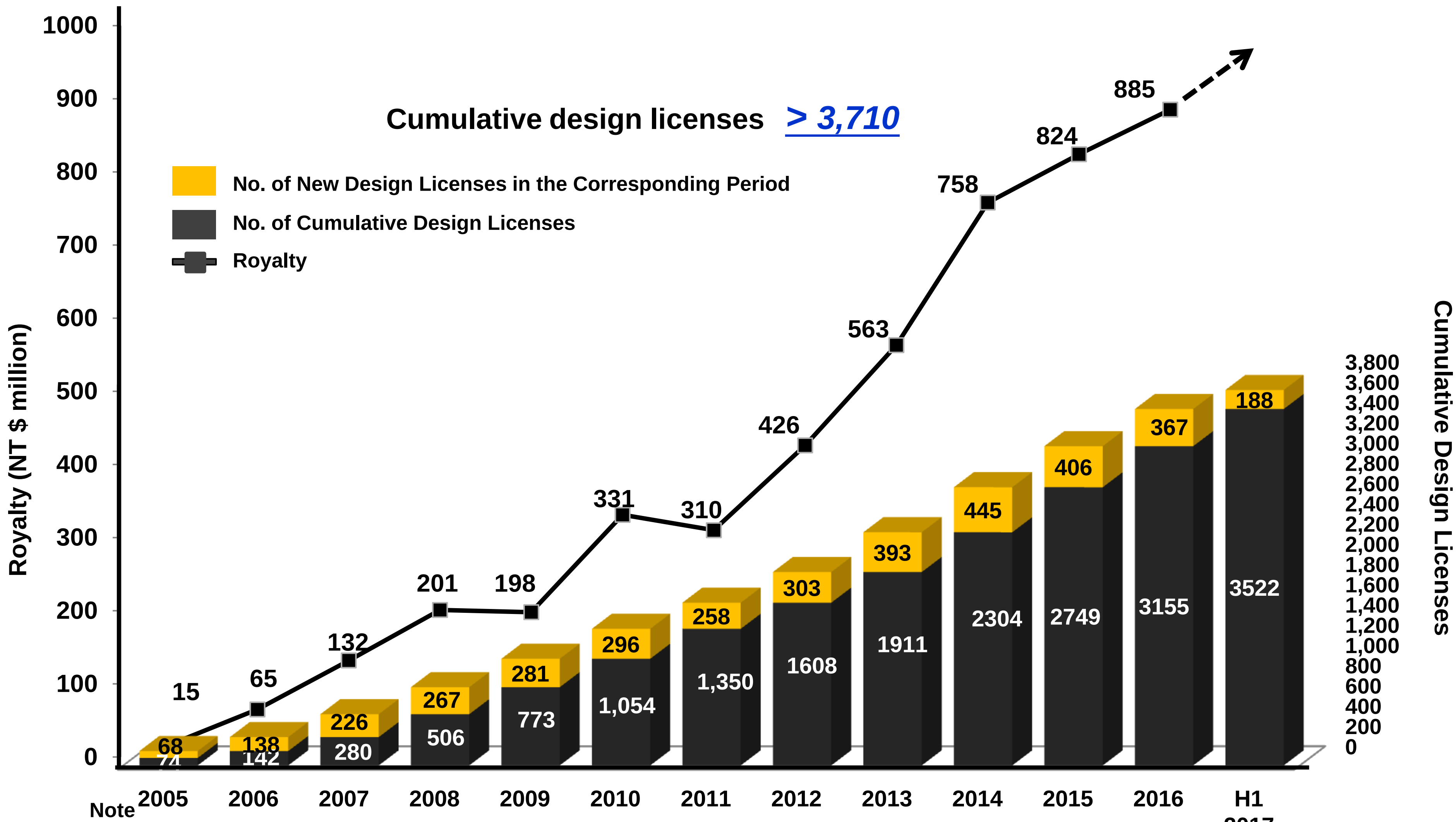
- A total* 188 NTO in H1 2017 *(367@2016, 406@2015, 445@2014, 393@2013)



	2012				2013				2014				2015				2016				2017	
	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2
NRE	7	15	10	10	7	14	18	12	33	12	22	15	21	17	10	9	12	14	18	12	8	13
Usage	62	68	63	68	73	69	88	112	90	86	88	99	82	87	76	104	63	94	81	73	88	79

Note*: As the applications of MCU at several foundries have gradually entered mass production, and the business model of the main foundry partner which provides green process has shifted to — eMemory licenses IP cell to the foundry for it to provide direct design service to customers — as the result, the new tape out number of MCU has been affected, but the royalty coming from IP cell usage continues to roll in.
In summary, even the new tape out number of MCU is lower than before; the corresponding wafer output and royalty continue to grow.

Cumulative Licenses Drive Future Royalties



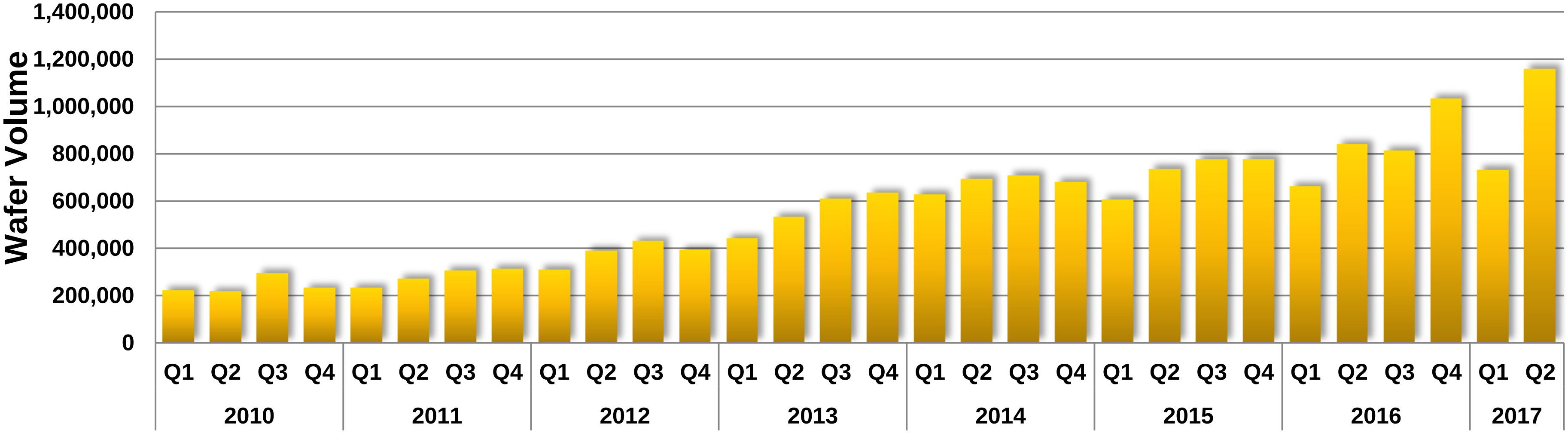
Note

1: Due to the 2009 recession, royalty income was down 1.5% from the previous year.

2: Prepaid royalty from a single customer contributed to 2010 annual growth of 67%, followed by a drop of 6.3% in 2011.

3: CAGR for 2009-2013 was 30%.

Wafer Production Volume



eMemory IP's Penetration Rates in T Company (in US$revenue)

	Process node	*% of T	Q2 17	Q1 17	2016	2015
8"	0.25/0.35	3%	44.84%	37.05%	28.15%	33.49%
	0.15/0.16/0.18	11%	7.36%	9.10%	12.43%	8.73%
	0.11/0.13	3%	58.76%	41.92%	42.61%	29%
12"	80/90nm	5%	12.73%	10.96%	12.50%	19.85%
	55/65nm	10%	4.73%	3.50%	3.59%	0.55%
	40/45nm	13%	0%	0%	0%	0%
	28nm	27%	0.18%	0.56%	0.55%	0.05%
	16/20nm	26%	0%	0%	0%	0%
8"		18%	21.77%	16.13%	18.86%	16.64%
12"		82%	1.43%	1.15%	1.44%	1.87%
Total		100%	5.07%	3.54%	4.27%	4.76%

* T company's Q2 2017 revenues broken down by process nodes

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eMemory's NVM Technologies

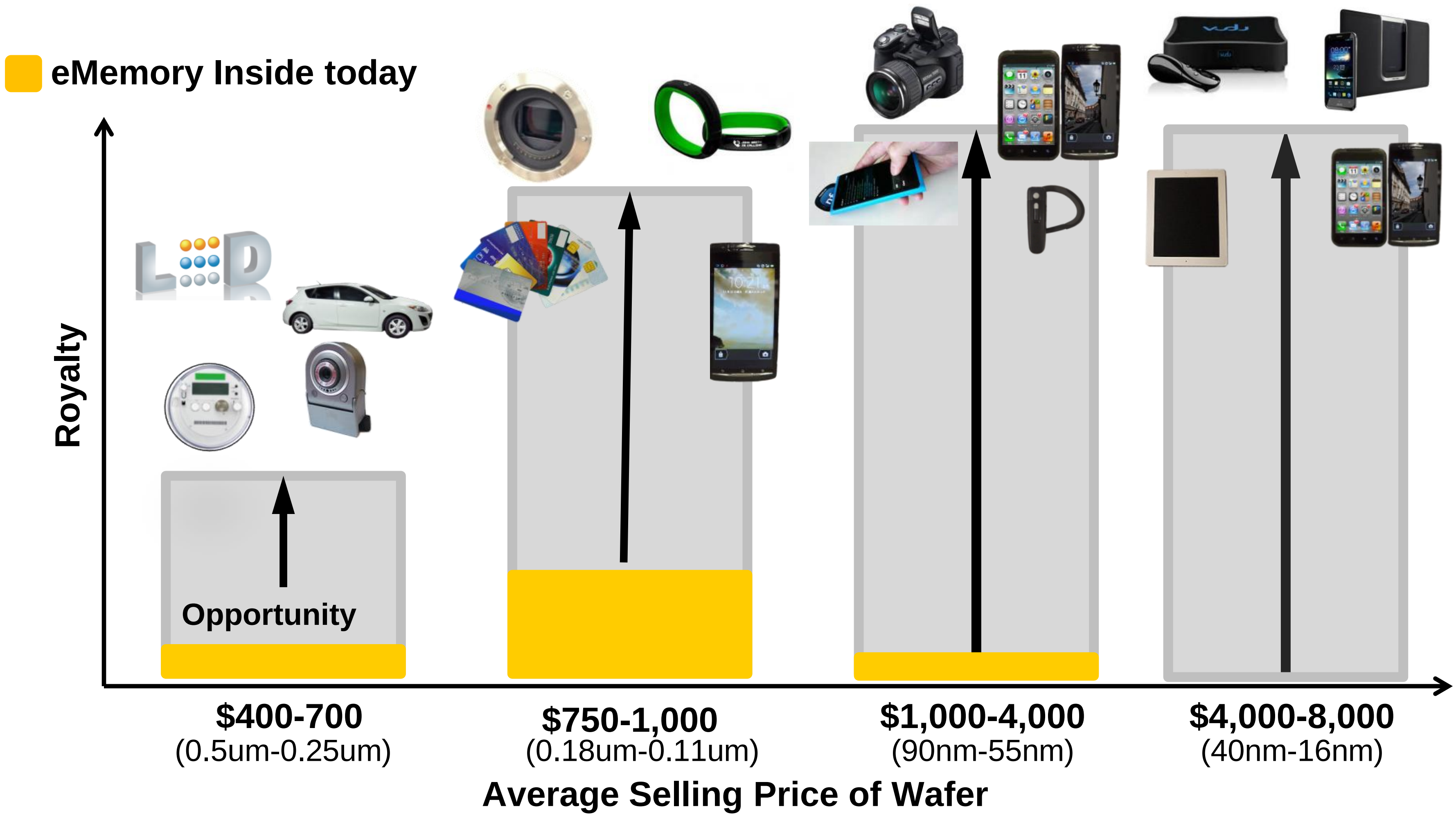
- **Logic NVM portfolio offers one-stop-shop solution.**
  - Compatible to any process
  - Robust structure
  - Low process cost
  - Competitive macro sizes
  - Easy integration
  - Easy porting

eMemory's NVM Technology	OTP			MTP	
	NeoBit	NeoFuse	NeoFlash	NeoEE	NeoMTP
Product Type	OTP	OTP	Flash	EEPROM	MTP
Endurance (Cycles)	10	10	1K~10K	10K~100K	1K~10K
Additional Mask Steps	0	0	2-3	0	0
Technology	Floating gate	Anti-Fuse	SONOS	Floating gate	Floating gate
Scalability	Simple	Simple	Simple	Simple	Simple
Memory Density	HD < 512Kb GHD < 16Mb	< 4Mb	< 2Mb	< 4Kb	< 512Kb

Applications by Technology

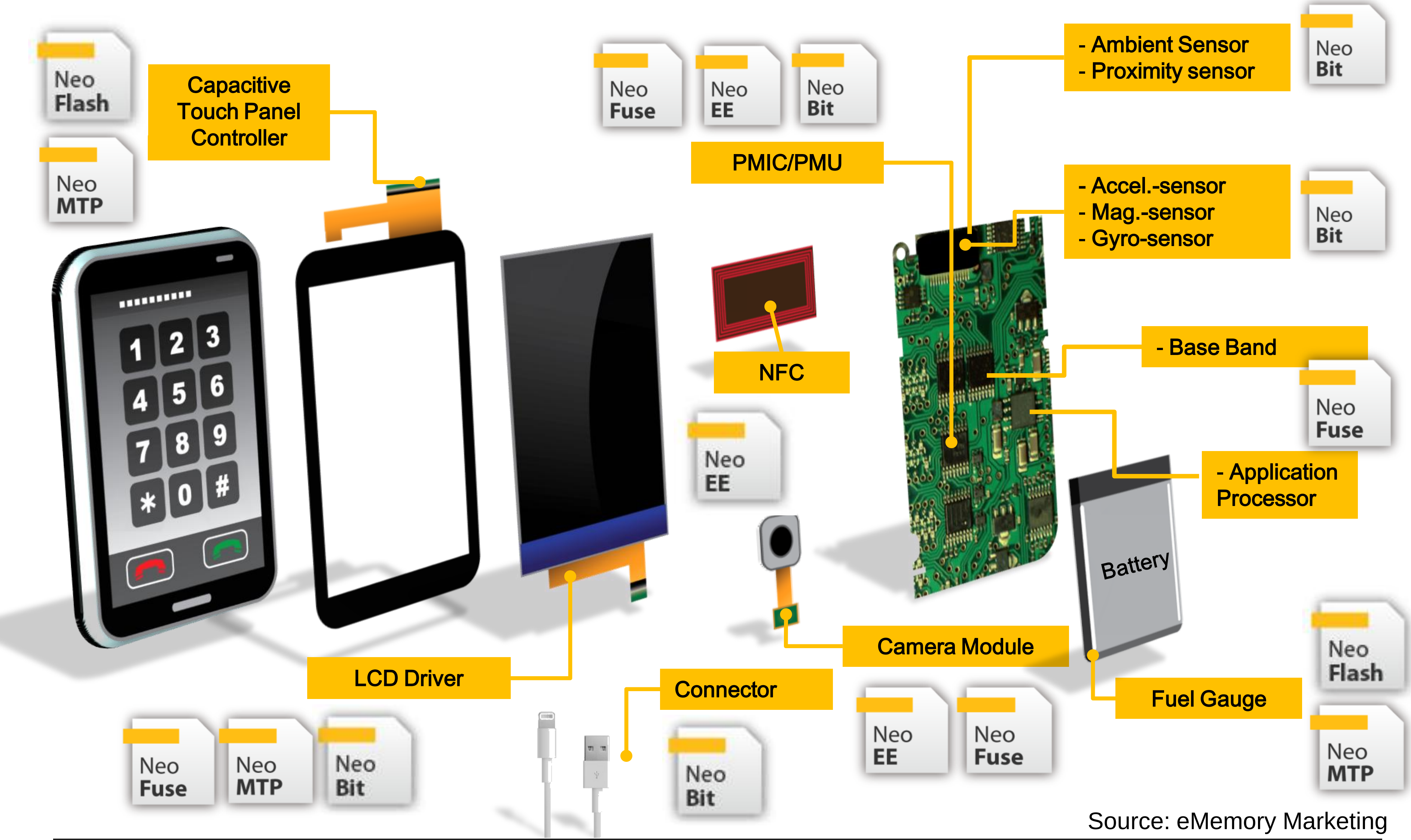
			12"					8"		
7nm	10nm	12/14/16nm	28nm	40nm	55/65nm	80/90nm	110/130nm	160/180nm	250nm	350nm

Opportunity at all Price Points



Note: 2.2 million 8" equivalent wafers with eMemory IP were shipped in 2013. (~5% of WW foundry shipment)

eMemory IP in Smart Phone



Source: eMemory Marketing

Benefits from Using eMemory IPs

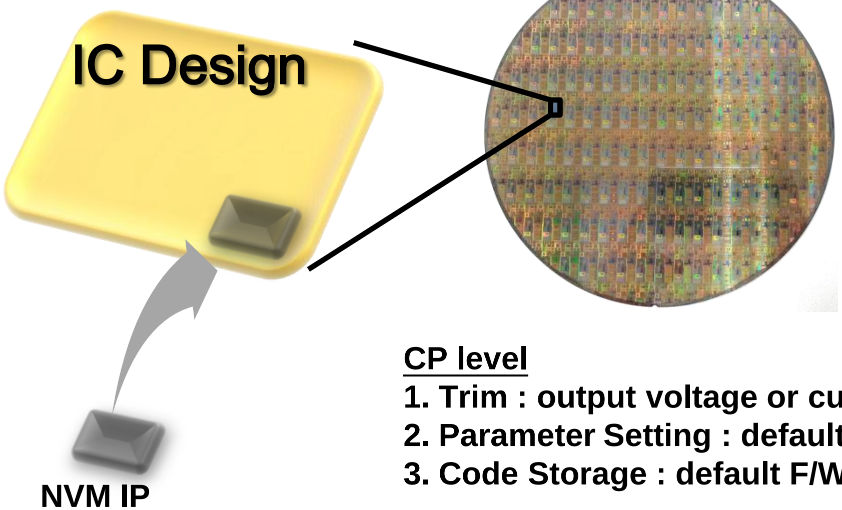
Package/FT level
1. Trim : SPEC shift
2. Parameter Setting : cross chip optimization
3. Identification Setting : manufacturer resume
4. Function Selection : setting for target market

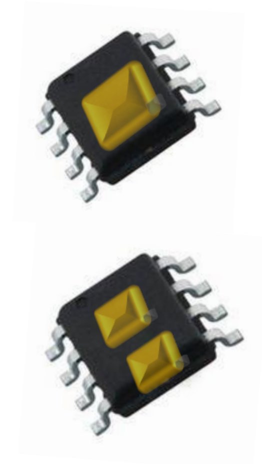
Design-in for
1. Trimming
2. Parameter Setting
3. Code Storage
4. Identification Setting
5. Encryption
6. Function Selection

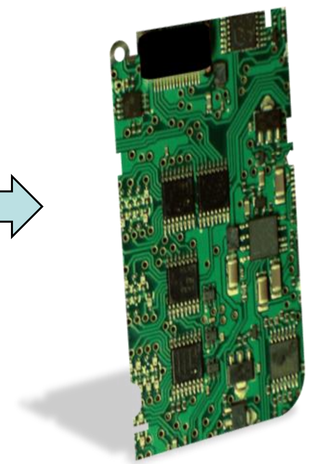
CP Test

Package/FT

System Assembling







CP level
1. Trim : output voltage or current
2. Parameter Setting : default value
3. Code Storage : default F/W code

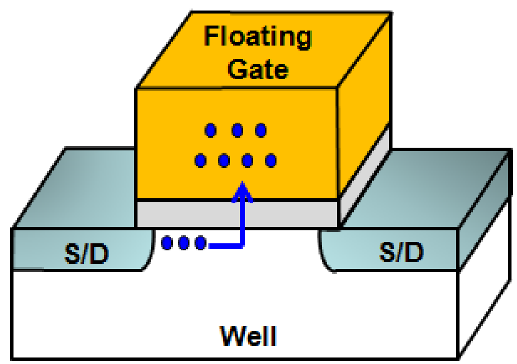
System Assembling
1. Parameter Setting : cross chip optimization
2. Code Storage : F/W code modification
3. Identification Setting : manufacturer resume
4. Encryption : Security algorithm or key storage

Invisibility for Security

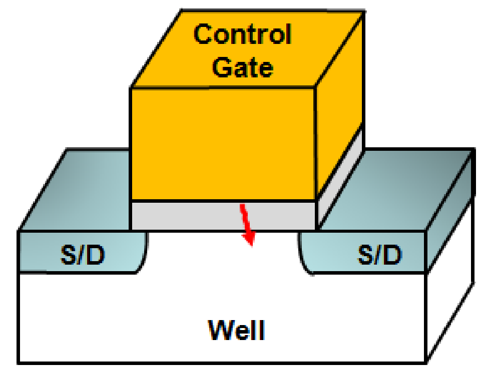
- Provide “Invisible Hardware Key” for invisible storage
- Prevent reverse-engineering to detect content of security key
- Protect firmware and hardware of ICs from pirating
- Extend & protect customer’s business

eFuse Key: Data is easily observed

Invisible Hardware Key : Data is hard to be detected



Floating Gate



Anti-Fuse

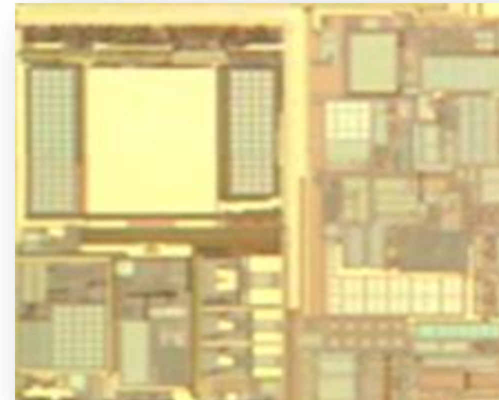
Security & Protection

Authorized Product

Fake Product

reverse copy

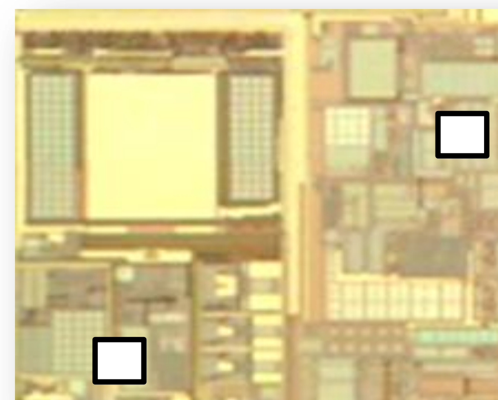
re-produce



without protection

reverse copy

re-produce

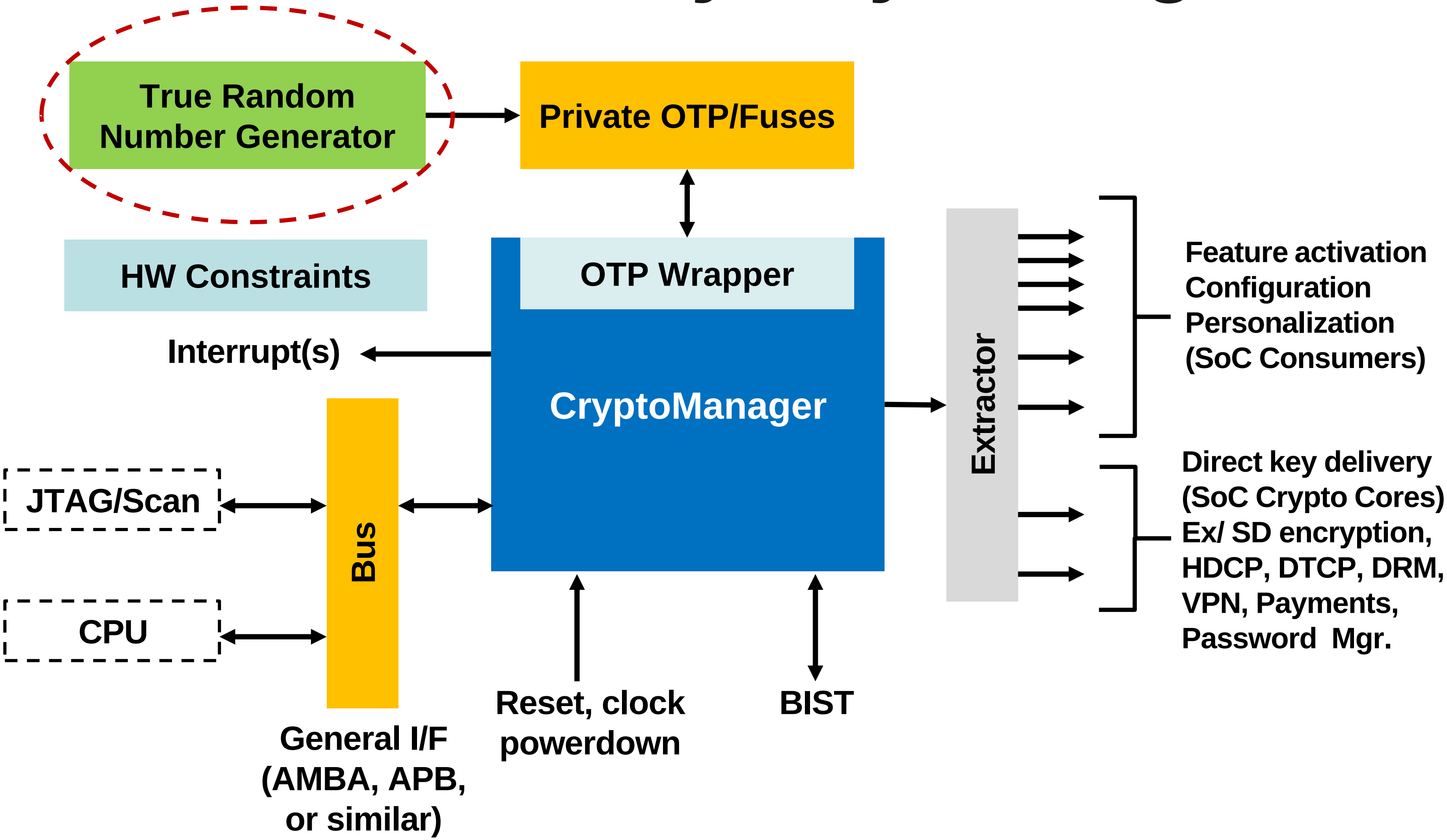


with protection

Security IP/Code by Authorized Use

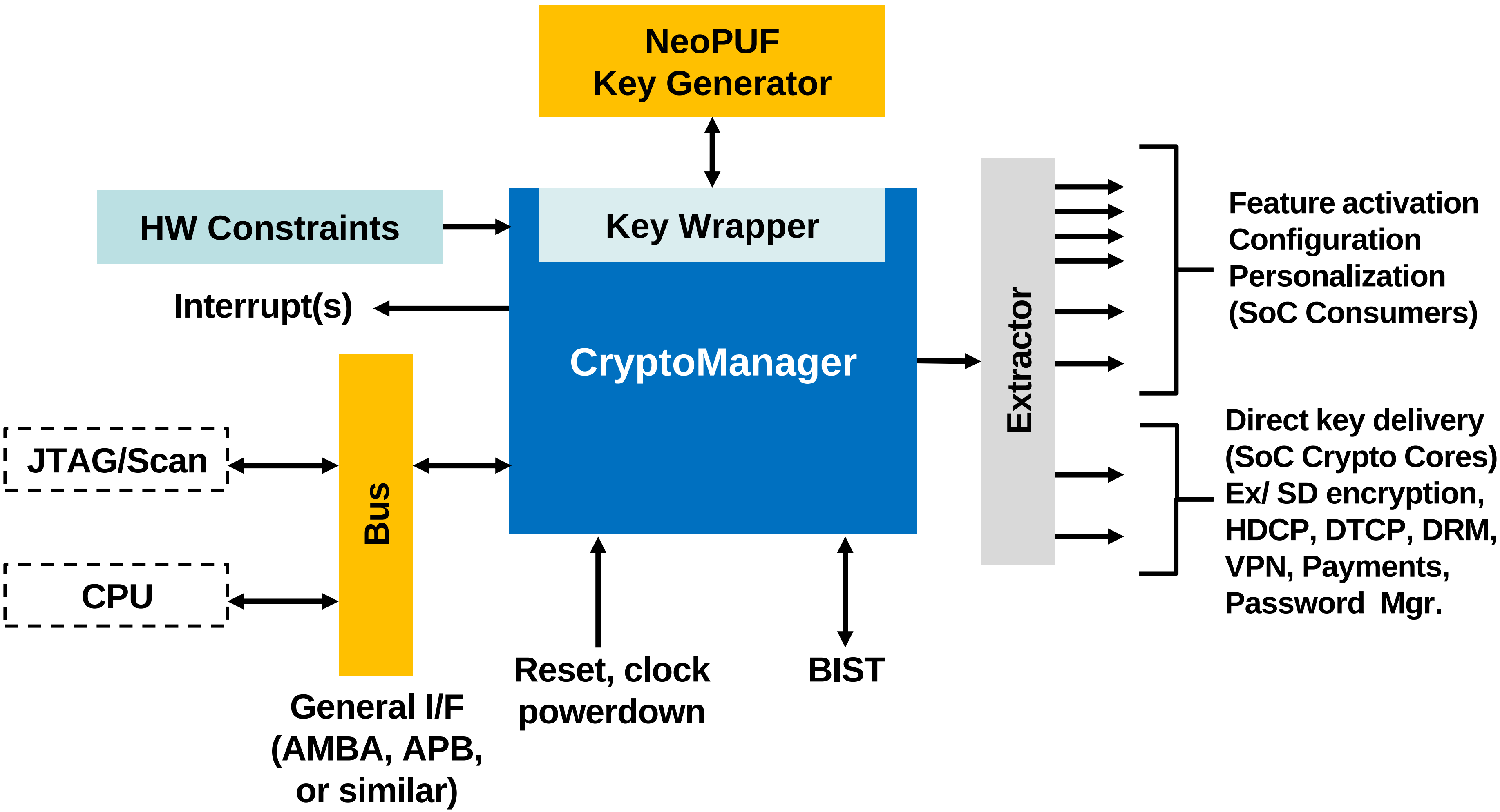
Can NOT Work w/o Security IP/Code

OTP for security Key storage



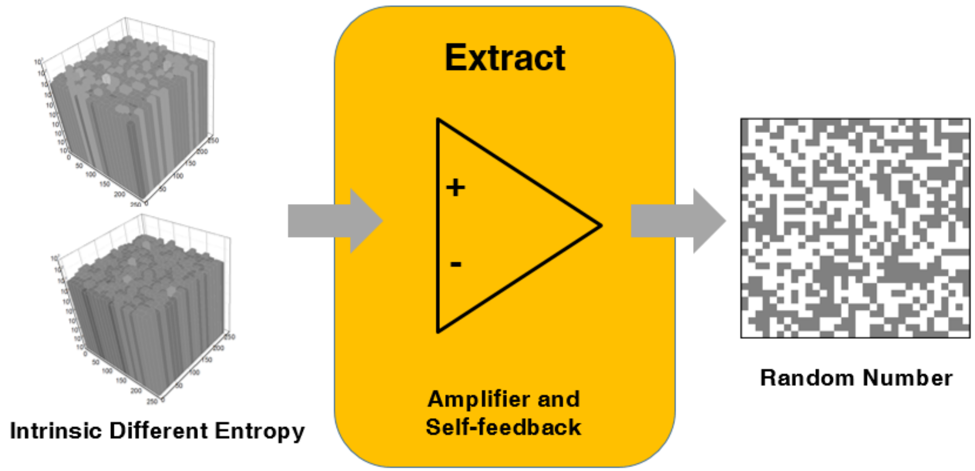
Source : Rambus crypto manager platform

NeoPUF for Security Key Generation



Source : Rambus crypto manager platform

What is <u>P</u>hysical <u>U</u>nclonable <u>F</u>unctions



Collision Probability $\fallingdotseq$ 1/15B $\fallingdotseq 1/2^{34}$

Collision Probability = $1/2^{\text{Bits Stream Length}}$

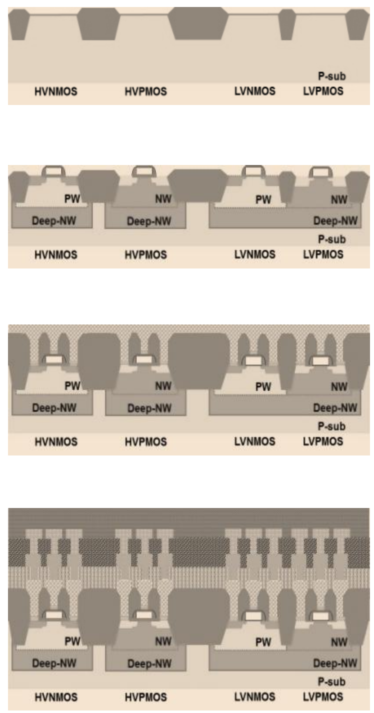
NeoPUF Technology

IC Design

eMemory IP

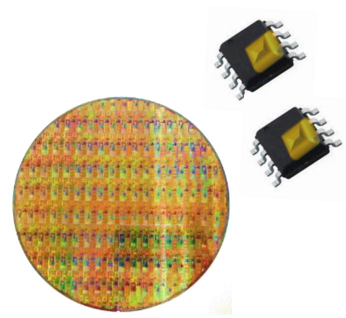
Design-in
Customized SPEC & Function are designed for customer demands

Wafer Process



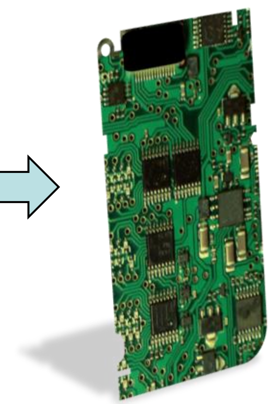
Manufacturing
Process Variation is introduced during manufacturing process (+0 mask logic process)

CP /FT Test



Product Testing
Random Noise is enhanced and generated randomly

System Assembling



System Assembling
Random Seed activates Identification, Encryption, Authentication, Security Key Storage

NeoPUF - Essential Security Component

- Unique & unclonable hardware root of trust
- Authentic random number generator
- Every chip equipped with its own “fingerprint”
- Multiple functions:
  - Encryption-decryption key to secure stored data
  - Public-Private key pair generation
  - Digital signature of hardware
  - Device secure booting

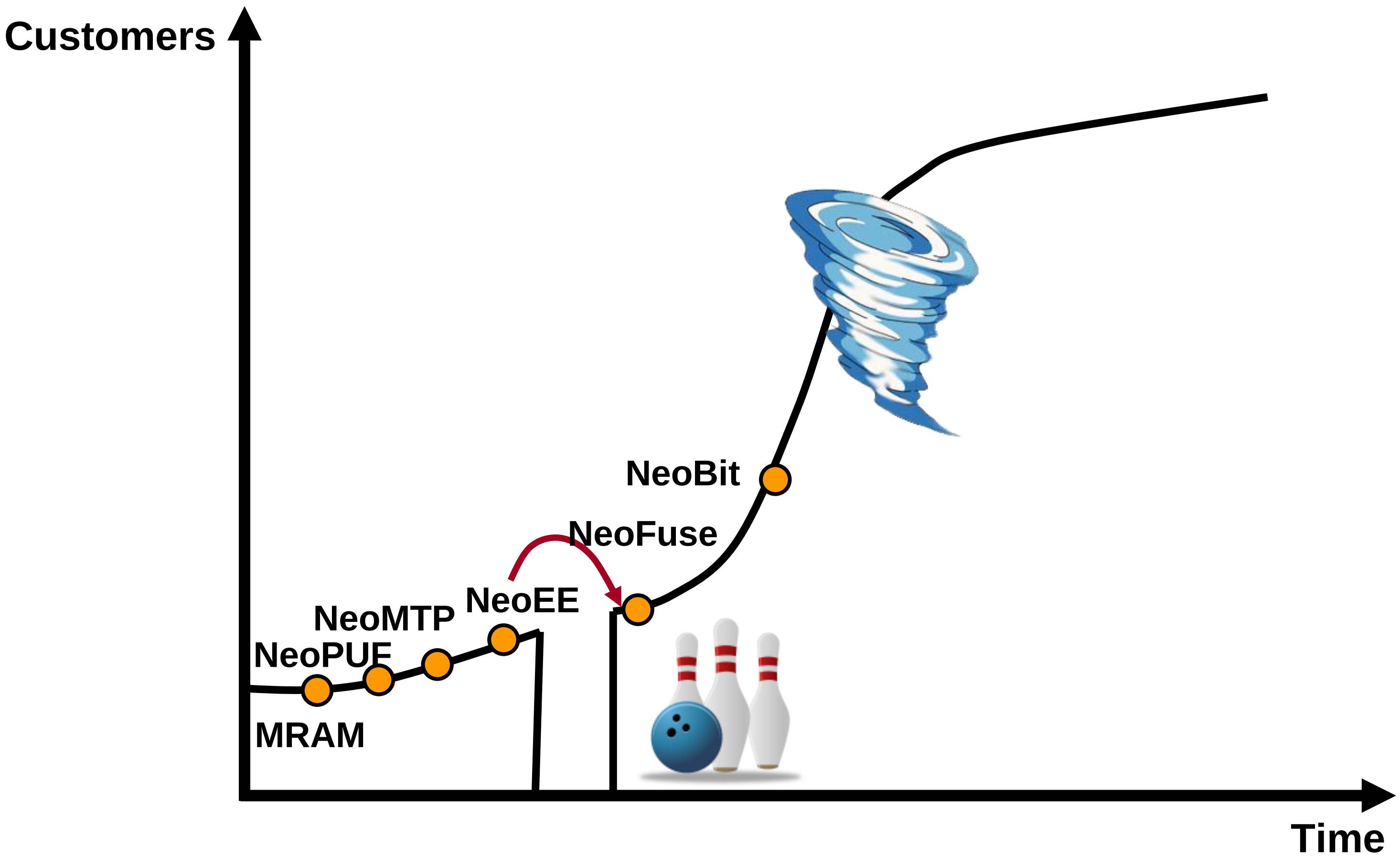
NeoPUF – Authentication & Security Everywhere

Smart Payment/IoT Device/Data Center

Data Storage Security

Hardware ID Tracking

Crossing the Chasm



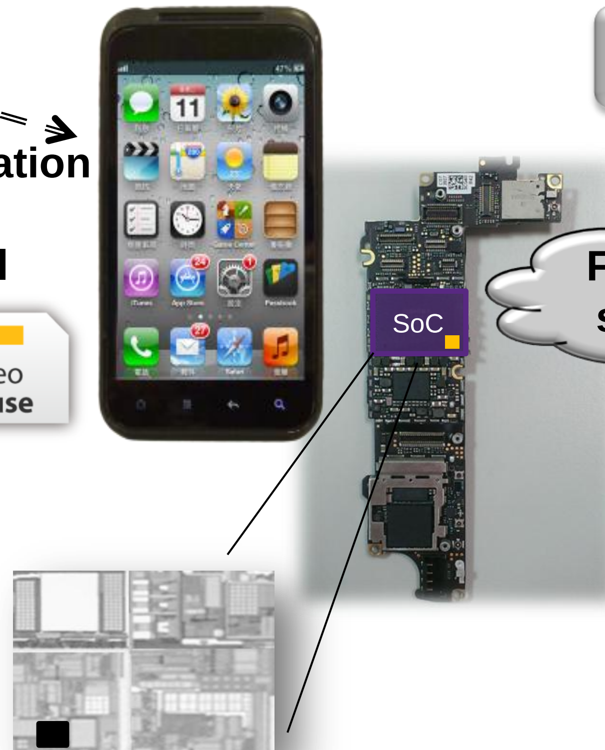
Security with eMemory IPs

Security for System Service

Cloud Processing

ID & Authentication
Data Integrity
Access Control

Neo EE　Neo Bit　Neo Fuse



Neo Fuse　Neo Bit

HW-SW/FW Lock

HW Key

Security Lock

FW (OS) with security key

HW Protection
Invisible Key for Anti-Cloning

Neo Fuse　Neo Bit

Security IP/Code by Authorized Use

NVM IP Demand in IoT

All Smart Systems

	Sensing	Embedded Processing	Connectivity
Basic Technology	Sensing	Embedded Processing	Connectivity

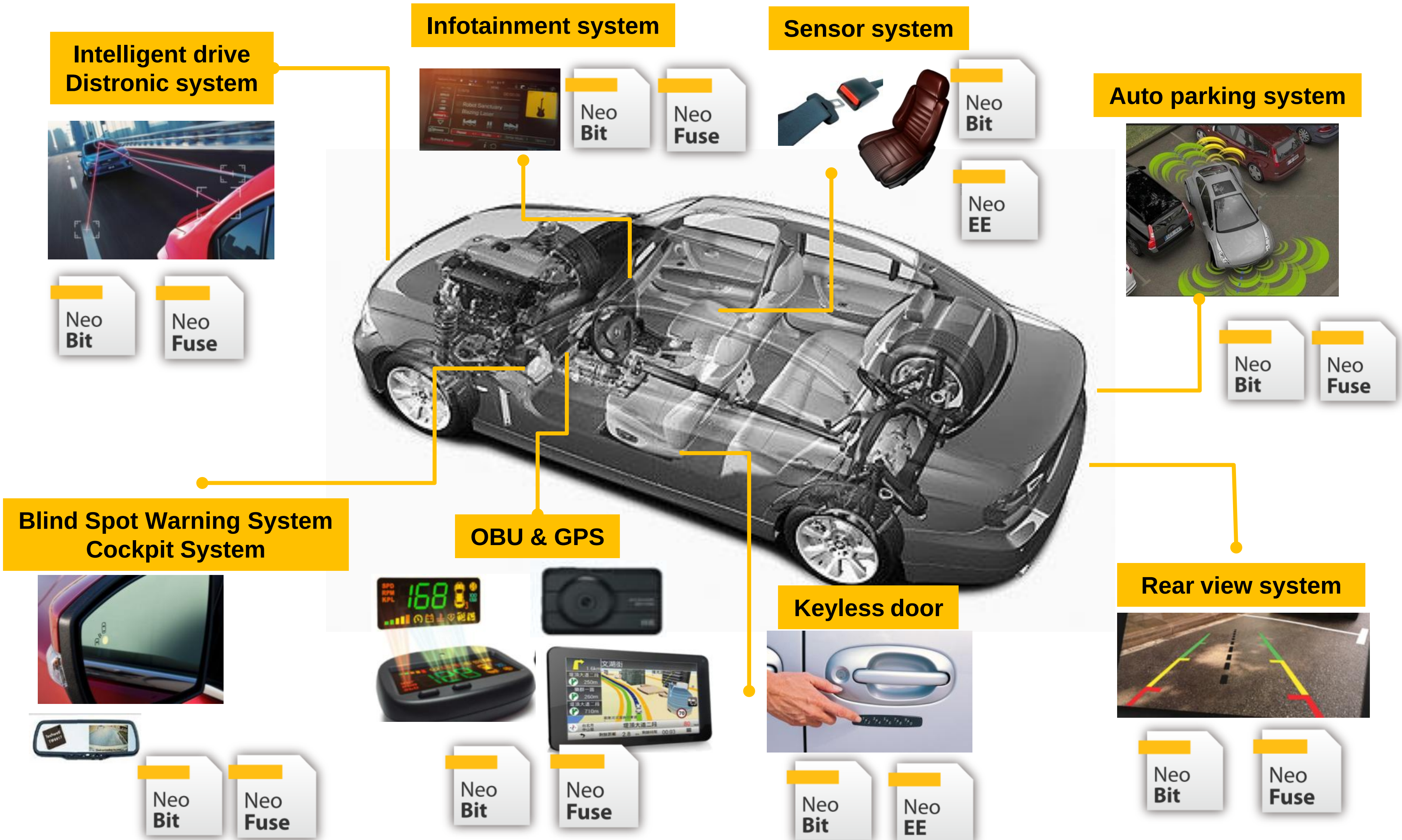
IC Types

- Sensing: Accelerometer, Magnetometer, Gyroscope, Pressure, Altimeter, Temperature
- Embedded Processing: MCU, MPU, Hybrid MCU/MPU, Network Processor
- Connectivity: NFC, Cellular, GPS, Sub-Gig, BT/BTLE, ZigBee, Wi-Fi, RFID

NVM IP Function

Encryption/Security	Function Selection	Trimming/Calibration
F/W code storage	Parameter Setting	ID Setting

Autotronics with eMemory IPs



Outlook for Q3 and beyond

Revenue growth to accelerate in H2 2017

- **Key drivers to licensing revenue:**
  - **Worldwide foundry partners keep developing advanced processes and MTP platforms.**
  - **We're establishing partnerships with more foundries worldwide.**
  - **Our growing IP library will also boost design license revenue.**

- **Key drivers to royalty revenue：**

  8-inch processes

  - **Fingerprint royalty grow explosively due to an expansion from high-end to mid-low smartphones markets as well as our market share gains.**

Outlook for Q3 and beyond

- **PMIC royalty will increase strongly with content increase of new smartphones. Growths will be driven by the ramp of new products by a US smartphone maker in H2, as well as a shift of business terms with the largest US chipmaker from "one-time fee" to "royalty-based".**
- **MTP IP series start contributing to royalty with more design-wins.**
- **Automotive applications start generating royalty.**

12-inch processes

- **With display technology migrating toward TDDI and OLED, our customers continue volume production of high-end TDDI (55nm) and OLED (40nm) products.**
- **STB, Multimedia and Network-related applications have been taped out subsequently in 28nm and below.**

Outlook for Q3 and beyond

- **R&D developments**
  - **Our IP has been taped out at 12nm and 22nm SOI process. The 7nm IP first taped out in April at one foundry, and one more tape-out expected in September at another foundry.**
  - **NeoPUF, our security IP, has been taped out at a major foundry and is to be designed into products by the end of this year.**
  - **Autotronic customers have started volume production beginning this year.**

Key Growth Drivers

Growth in application per mobile devices	• More chip applications per smartphone/tablet product.
Growth into more markets	• From consumer electronics and mobile devices to wearable devices. • Adding new NVM product lines further enable more product applications.
Growth in advanced technology	• Higher royalty per wafer is contributed from more advanced technology nodes.
Great IoT era	• Embedded Logic NVM will be a must.

Q & A

ememory

Embedded Wisely, Embedded Widely