A Leading Logic NVM Company

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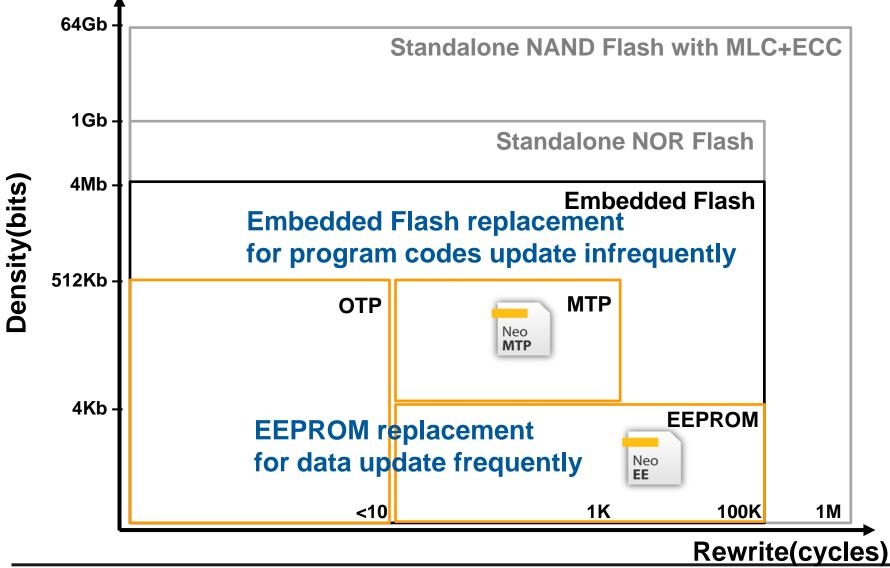


Outline

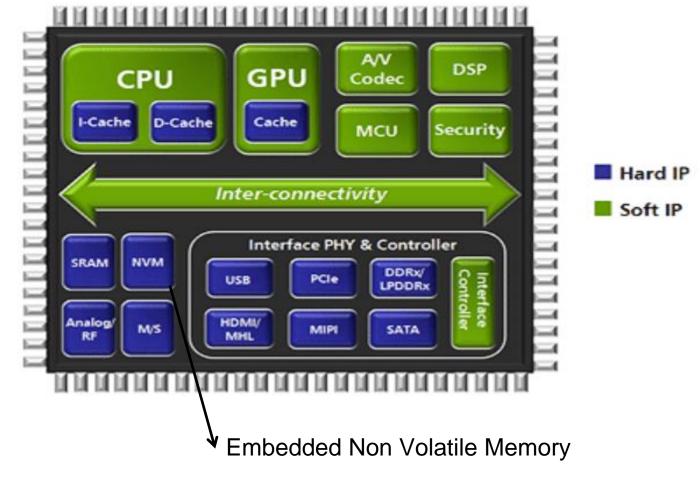
Business Model

- Review of Operations
- Growth Opportunity and Future Outlook
- Q & A

Nonvolatile Memory Classifications



SOC Block Diagram



Source : tsmc



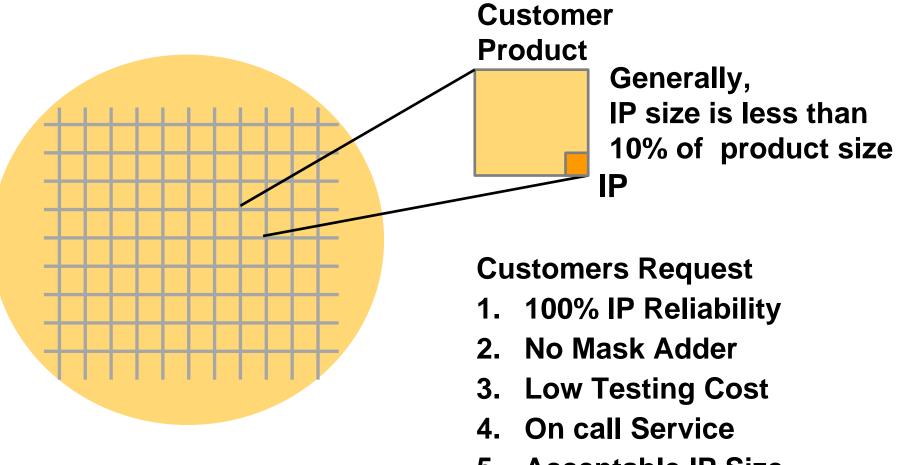
Embedded NVM Technologies

	ROM	eFuse (OTP)	Antifuse (OTP)	CMOS Floating Gate (OTP)	CMOS Floating Gate (MTP)	Embedded Flash
Cell Structure	Transistor	Poly Fuse	Antifuse	Floating Gate	Floating Gate	Floating Gate
Standard CMOS Compatible	Yes	Yes	Yes	Yes	Yes	No
Bitcell Area	< 1	50	1	2	4	1
Endurance	Νο	No	< 10	< 10	10K-100K	100-1000K
Density	4Kb-1Mb	256bit-4Kb	16bit-1Mb	16Kb-1Mb	1Kb-2M	64Kb-4Mb
Security	Low	Low	High	High	High	High
Additional Steps	None	None	None	None	None	+10 Mask

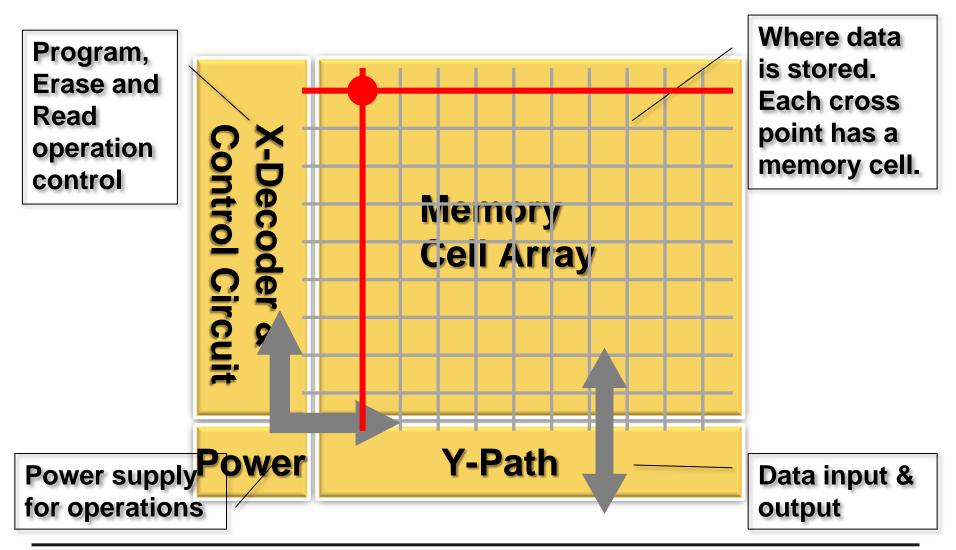
ROM not programmable, eFuse cannot scale beyond 16Kb, embedded flash expensive and cannot scale after 40 nm

• eMemory's IPs: OTP (antifuse, floating gate) and MTP (floating gate)

Considerations for IP Adoption

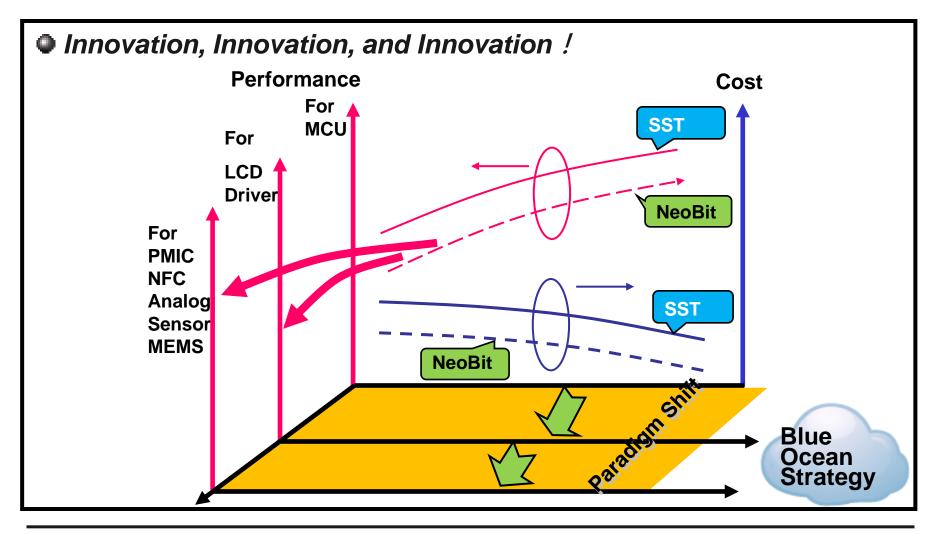


Inside Nonvolatile Memory IP



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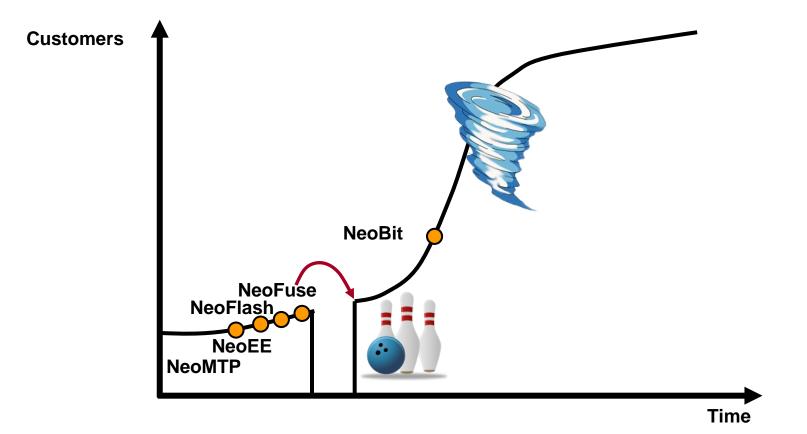
What We Have Done



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Crossing the Chasm



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2016 Technology Development

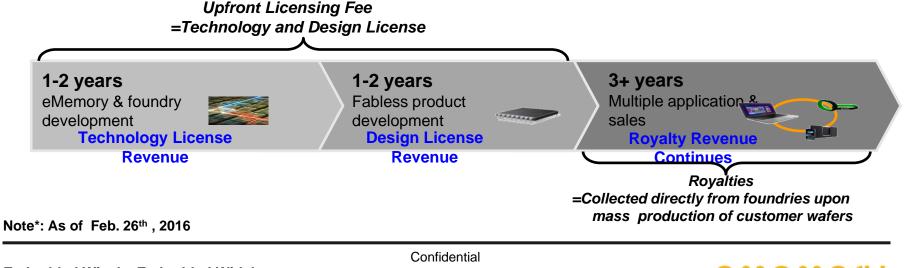
	Mass Production	Qualification	IP develop.	Device develop.
	0.6um-0.11um logic process	0.11um auto HV process		
	0.25um-0.13um BCD process			
	0.18-0.13um auto BCD process			
NeoBit	0.35um-55nm HV process			
NEODIT	0.18um auto HV process			
	3.3V & 5V green shrink version			
	0.11um CIS process			
	0.18um SiGe process			
	16nm FF+/FFC process	10nm FF process	7nm FF process	
	28nm HPM/ HPC+ process	65nm CIS Process	14nm FF process	
	55-28nm LP process			
	55-28nm ULP process			
NeoFuse	90-40nm HV process			
Neoruse	130-55nm eFlash			
	63nm DRAM process			
	0.15/0.13um BCD process			
	0.11um/55nm CIS process			
	0.15um no MV process			
	0.11um RFID	0.11um BCD process	0.18um LP process	
	0.11um Logic process			
	0.13/0.11um LP process			
NeoEE	0.18-0.153um logic process			
	0.18um 3.3V;5V Green process			
	0.3/0.18/0.13um BCD process			
	0.18um auto BCD process			
	110-55nm HV process		55nm HV (shrink)	
	0.11um/0.18um logic process			
NeoMTP	0.153um/0.18um 3.3V;5V Green			
	process			
	0.13 um/0.18um BCD			
	0.18um logic process			
NeoFlash	0.18/0.16um HV process			
	0.11um logic process			

Business Model

- Founded in 2000. First customer engaged in 2002. Achieved profitability in 2005 and IPO in 2011. The largest logic non-volatile memory IP company, 225 employees (157 R&D)*.
- Since its IPO, the company initiated no new fund raising or bank debt, and has distributed in excess of 100% of earnings in cash dividends.
- Growth Indices: 1) No. of on-going technology platforms

2) No. of design licenses

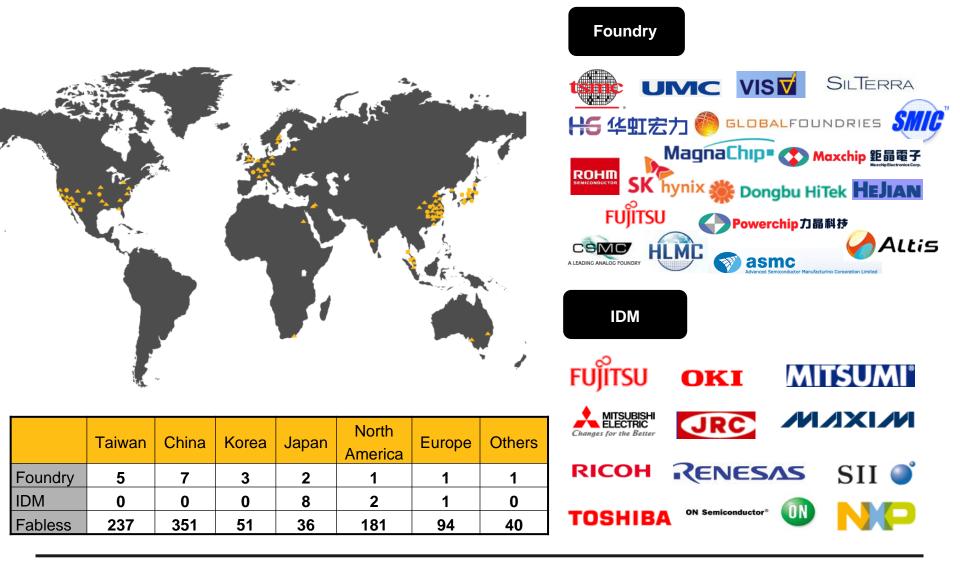
3) Royalty



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Worldwide Customers



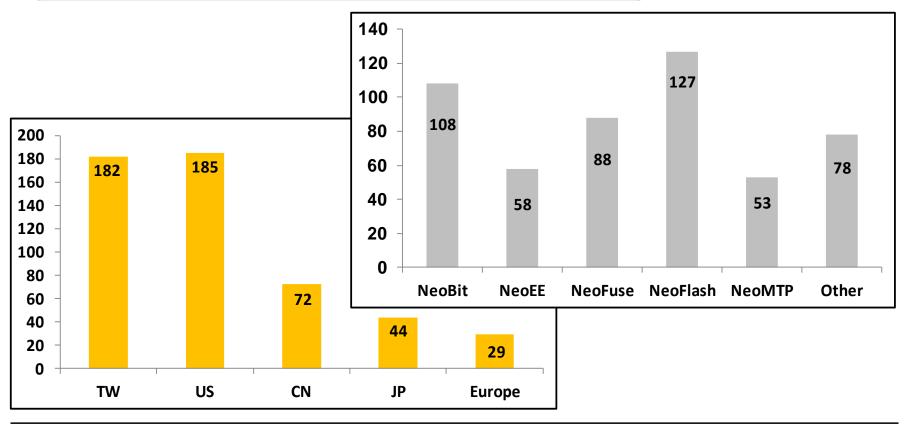
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Patent Portfolio

	Q3 15	Q4 15	Diff.
Pending	187	187	-
Issued	304	325	+21
Total	491	512	+21



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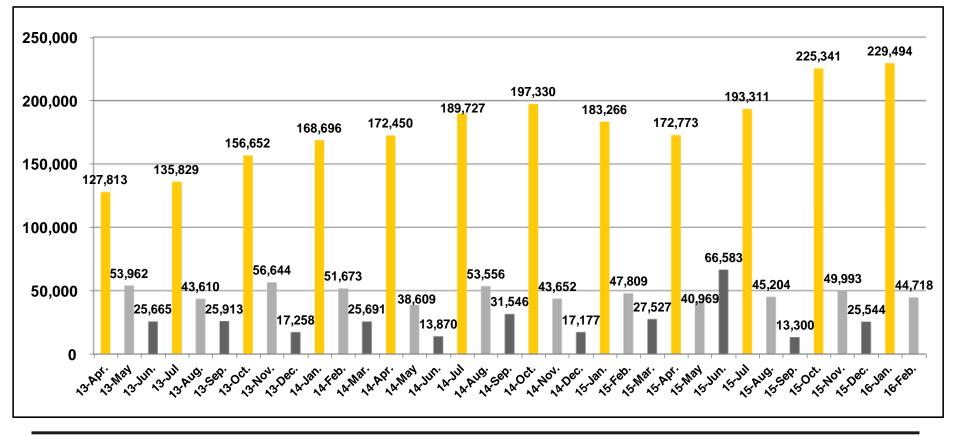
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Quarterly Revenue Pattern

• The quarterly royalty from most of foundries are collected at first month of each quarter and from some other foundries are collected at second month, and none at third month.

Unit : NTD Thousands



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Q4 Revenue Breakdown

Unit: NTD thousands

	2015 Q4	2015 Q3	QoQ	2014 Q4	ΥοΥ	2015	2014	YoY
Licensing	69,307	38,167	81.59%	51,849	33.67%	267,512	246,073	8.71%
Royalty	231,571	213,648	8.39%	206,310	12.24%	824,108	757,904	8.74%
Total	300,878	251,815	19.48%	258,159	16.55%	1,091,620	1,003,977	8.73%

Unit: Number of contracts

		2015 Q4	2015 Q3	2015	2014
Technology Licenses		11	4	28	21
Design NRE		9	10	57	82
Licenses	Usage	104	76	349	363



Financial Income Statement

(Unit: NTD thousands)	Q4 15	Q4 14	% change	2015	2014	% change
Revenue	300,878	258,159	16.5%	1,091,620	1,003,977	8.7%
Gross Margin	100%	100%	-	100%	100%	-
Operating Expenses	156,216	148,466	5.2%	570,403	540,286	5.6%
Operating Margin	48.1%	42.5%	+5.6ppts	47.7%	46.2%	+1.5ppts
Net Income	128,090	100,931	26.9%	479,111	418,604	14.5%
Net Margin	42.6%	39.1%	+3.5ppts	43.9%	41.7%	+2.2ppts
EPS (Unit: NTD)	1.69	1.33	27.1%	6.32	5.52	14.5%
ROE	28.4%	23.4%	+5.0ppts	26.6%	24.3%	+2.3ppts

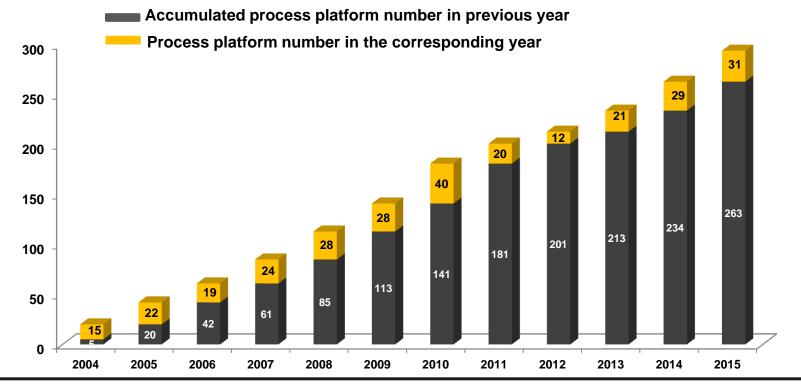
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Technology License

Unit: Number of contract

Year	2013	2014	2015
License number	19	21	28

Note: The terms (including number of process platforms and licensing fees) for each technology license are set contractually. Payments are made according to set milestones, and there are no particular seasonal factors involved.



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Current Technology Development Platforms

- Total (As of Dec.) : 100
- 16 for NeoBit, 38 for NeoFuse, 26 for NeoEE, and 20 for NeoMTP.

	10nm	14/16nm	28nm	40nm	55/65nm	80/90nm	0.11~ 0.13um	0.15~ 0.18um	>0.25 um	Total
NeoBit	-	-	-	-	-	-	5	11	-	16
NeoFuse	1	3	9	4	9	3	6	3	-	38
NeoFlash	-	-	-	-	-	-	-	-	-	0
NeoEE	-	-	-	2	-	1	6	17	-	26
NeoMTP	-	-	-	1	2	2	4	11	-	20

Current Technology Development Platforms

12" Fabs	Production	Development	NVM Type	Process Type
10nm	0	1	ОТР	FF
14/16nm	0	3	ΟΤΡ	FF+
28nm	5	9	ОТР	LP/HPM, HLP/HPM, LPS
40nm	2	7	OTP, MTP	HV-DDI, LP
55/65nm	10	11	OTP, MTP, Flash	LP, HV-DDI, HV-OLED, DRAM, CIS
80/90nm	5	6	OTP, MTP	HV-DDI, HV-OLED, LP
0.13/0.11um	6	4	OTP, Flash	HV-DDI, BCD, Generic
0.18um	1	0	ОТР	BCD

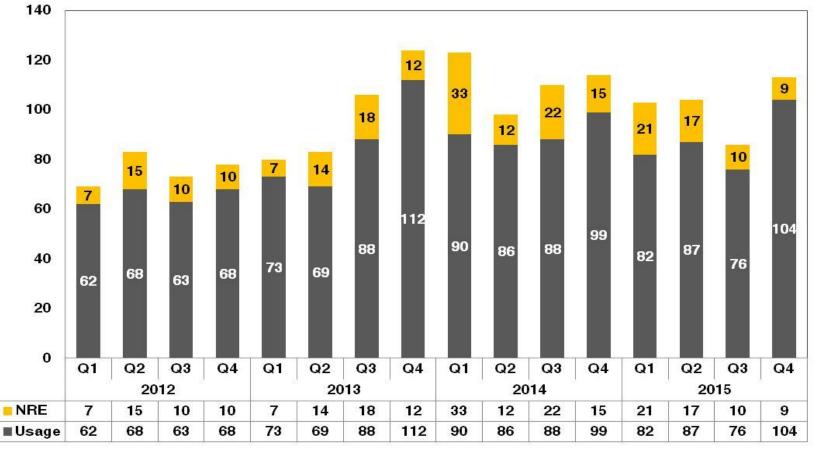
8" Fabs	Development	NVM Type	Process Type
0.13/0.11um	17	OTP, MTP, Flash	HV-DDI, BCD, LP, RF, CIS, LL
0.18/0.16/0.152um	42	OTP, MTP	Generic, LP, LL, MR, HV, Green, BCD
0.25um	0	OTP, MTP	BCD
0.35um	0	ОТР	UHV

*As of Dec. 31, 2015



Quarterly Design Licensing (New Tape Out)

- Total 406 NTO in 2015 (445@2014 393@2013, 303@2012, 258@2011)

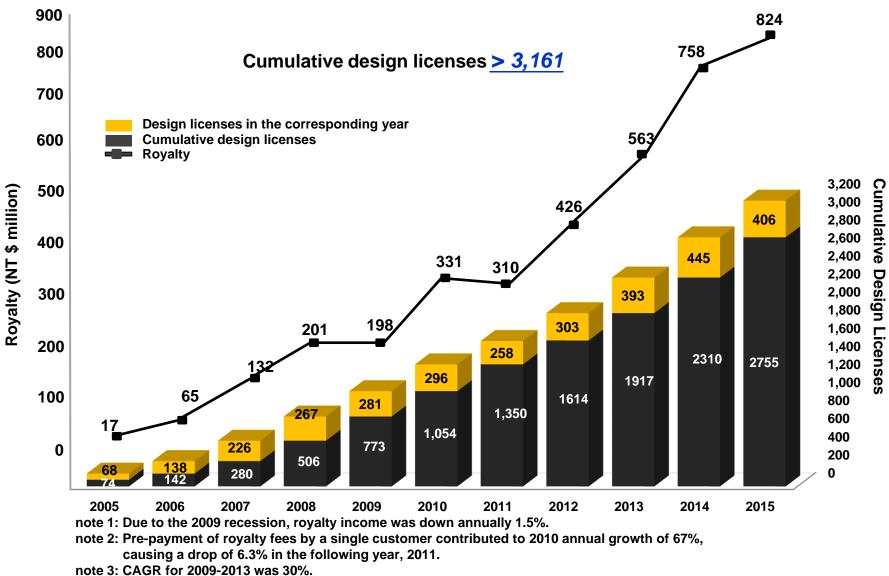


Usage : Usage of pre-qualified and verified IP (charged by per product tape out or annual package), the cycle time from design implementation to royalty payments for mass production is faster, typically less than one year. NRE: NRE covers the customization of IP that must undergo new verification or qualification. It typically requires 1 to 1.5

years before resulting in royalty revenue.

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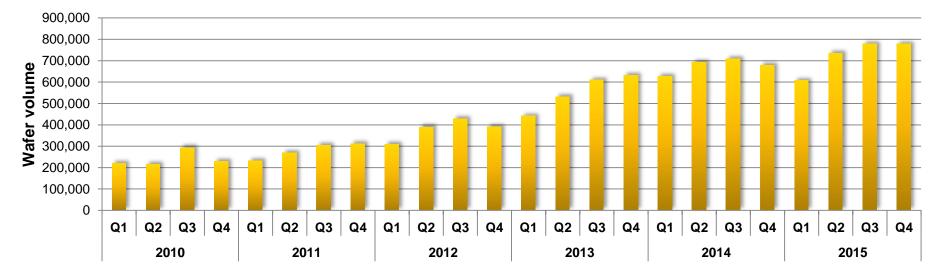
Cumulative Licenses Drive Future Royalties



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Wafer Production Volume



embedded eMemory IP in T Company (\$revenue); * % of Process node in T company total revenue in Q4 15

	Process node	*% of T	Q4 15	Q3 15	2015	2014
8"	0.25/0.35	4%	47.61%	38.2%	33.49%	30.5%
	0.15/0.18	11%	10.11%	7.9%	8.73%	11.9%
	0.11/0.13	3%	29.24%	30.9%	29%	20.8%
12"	90nm	7%	20.20%	21.8%	19.85%	16.3%
	65nm	11%	0.61%	0.9%	0.55%	0%
	40/45nm	14%	0%	0%	0%	0%
	28nm	25%	0.18%	0.02%	0.05%	0%
	16/20nm	24%	0%	0%	0%	0%
8"		19%	21.64%	16.3%	16.64%	15.6%
12"		81%	1.88%	2.3%	1.87%	1.4%
Total		100%	5.42%	5.0%	4.76%	4.5%

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eMemory's NVM Technologies

Logic NVM portfolio offers one-stop-shop solution.

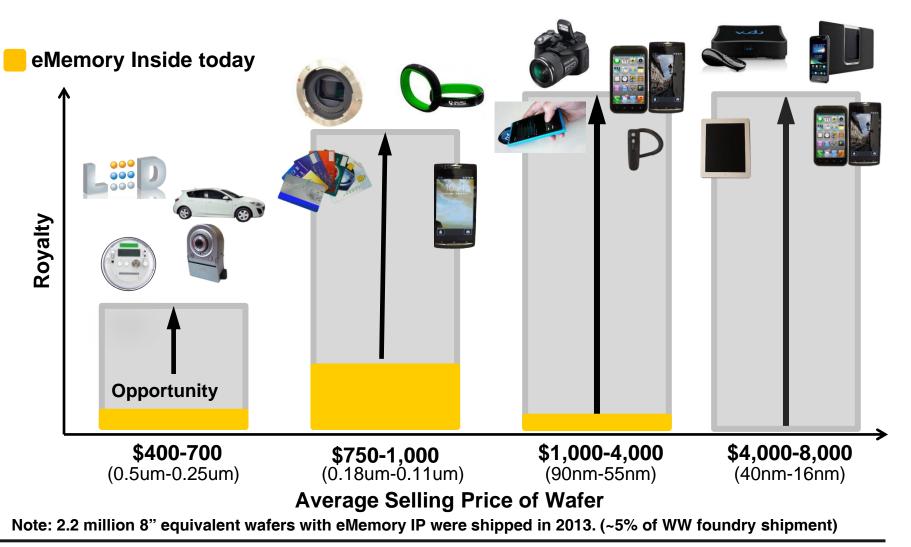
- Compatible to any process
- Robust structure
- > Low process cost

- > Competitive macro sizes
- > Easy integration
- > Easy porting

eMemory's NVM	07	ГР	МТР			
Technology	NeoBit	NeoFuse	NeoFlash	NeoEE	NeoMTP	
Product Type	OTP	OTP	Flash	EEPROM	MTP	
Endurance (Cycles)	10	10	1K~10K	10K~100K	1K~10K	
Additional Mask Steps	0	0	2-3	0	0	
Technology	Floating gate	Anti-Fuse	SONOS	Floating gate	Floating gate	
Scalability	Simple	Simple	Simple	Simple	Simple	
Memory Density	HD < 512Kb GHD < 16Mb	< 4Mb	< 2Mb	< 4Kb	< 512Kb	

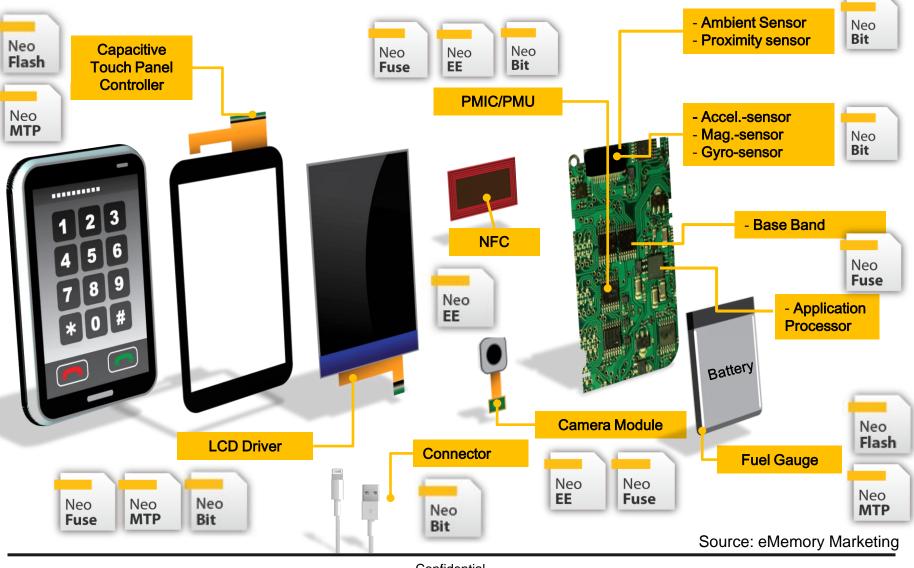


Opportunity at all Price Points





eMemory IP in Smart Phone

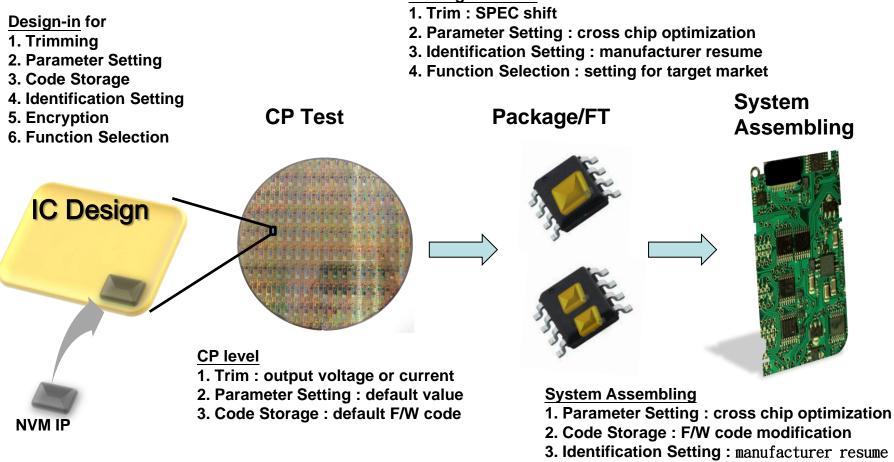


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Benefits from Using eMemory IPs

Package/FT level



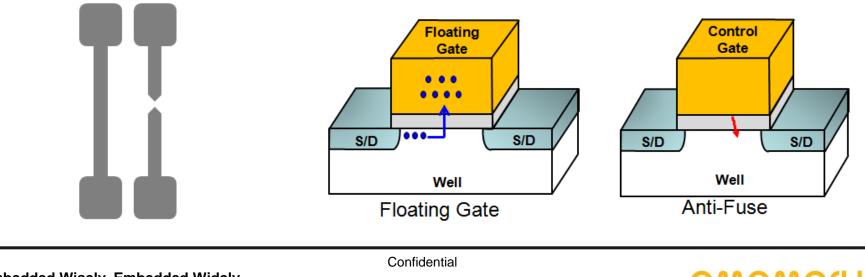
4. Encryption : Security algorithm or key storage

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Invisibility for Security

- Provide "Invisible Hardware Key" for invisible storage
- Prevent reverse-engineering to detect content of security key
- Protect firmware and hardware of ICs from pirating
- Extend & protect customer's business



Invisible Hardware Key : Data is hard to be detected

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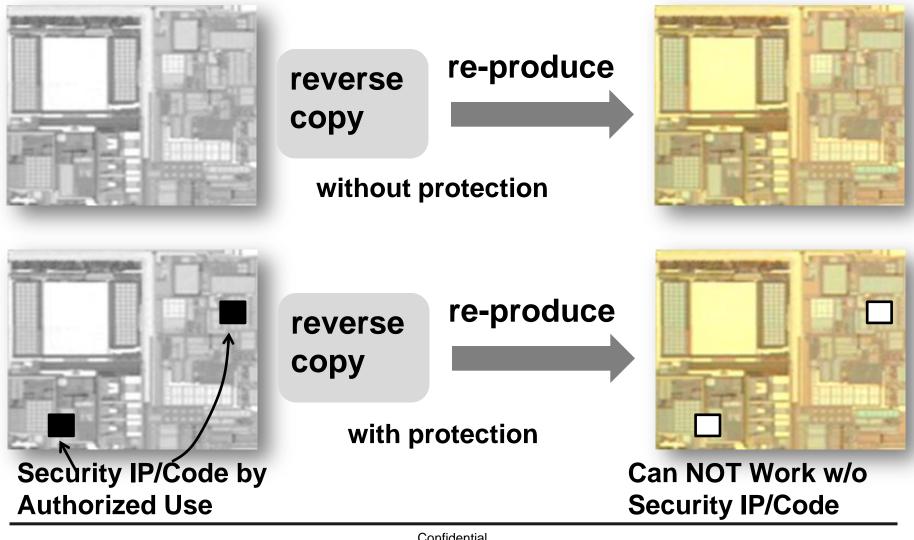
eFuse Key: Data is easily observed

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Security & Protection

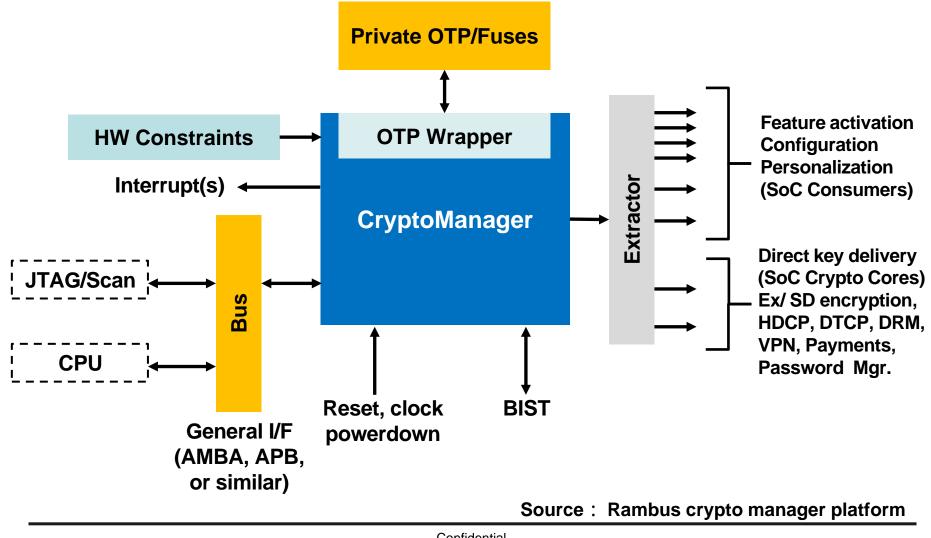
Authorized Product

Fake Product



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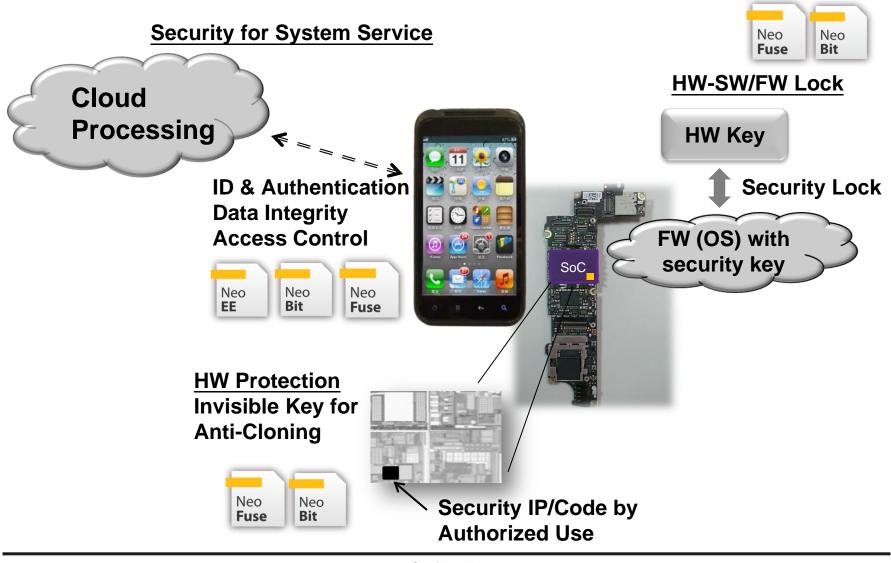
OTP for security storage



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Security with eMemory IPs

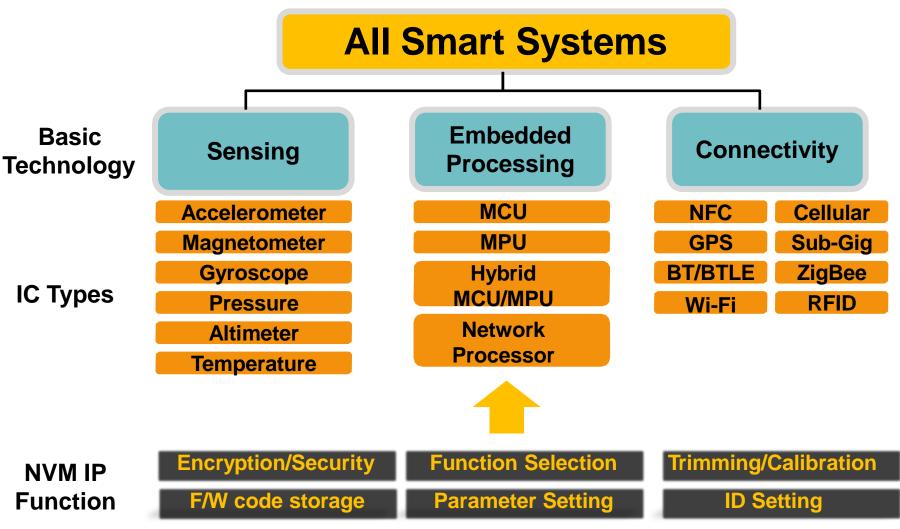


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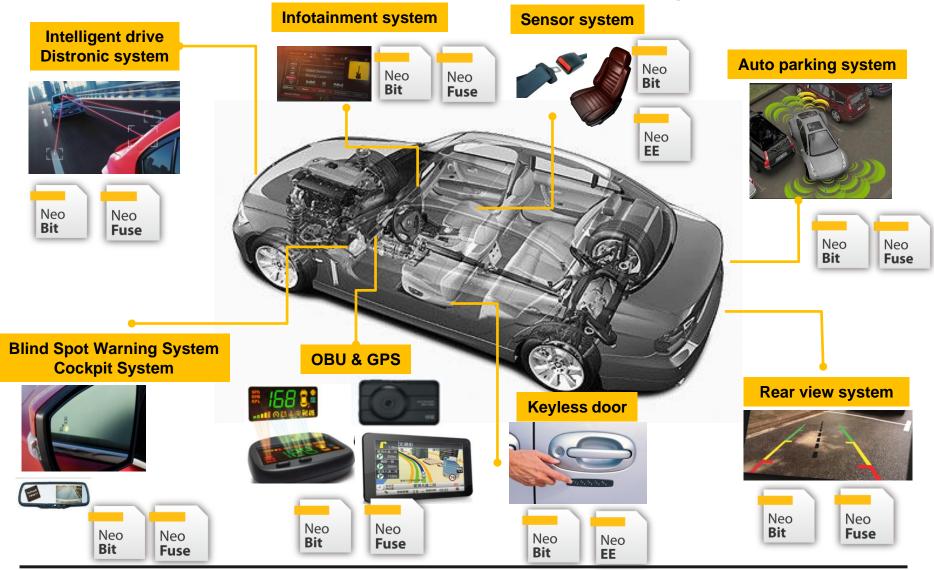
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NVM IP Demand in IoT



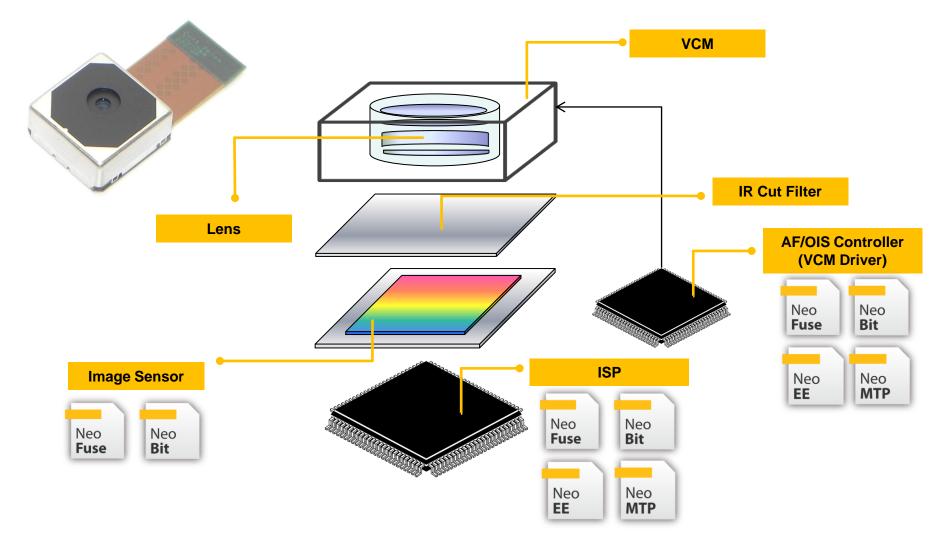
Autotronics with eMemory IPs



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Imager Module with eMemory IPs

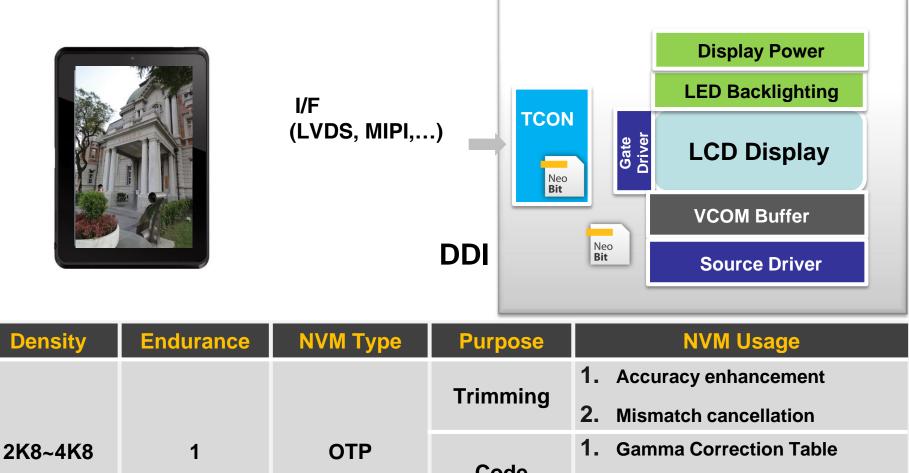


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Advanced LCD Driver ICs

Process Technology : 0.11um HV/80nm HV/55nm HV



Code	2 Timing Control Pottorn
Storage	2. Timing Control Pattern
5	3. Color Engine Enhancement

Power Management ICs for Baseband and Application Processor

Process Technology : Advanced 0.25um BCD/ 0.18um BCD/ 0.13um BCD Mature 0.18um/0.16um/0.152um Logic

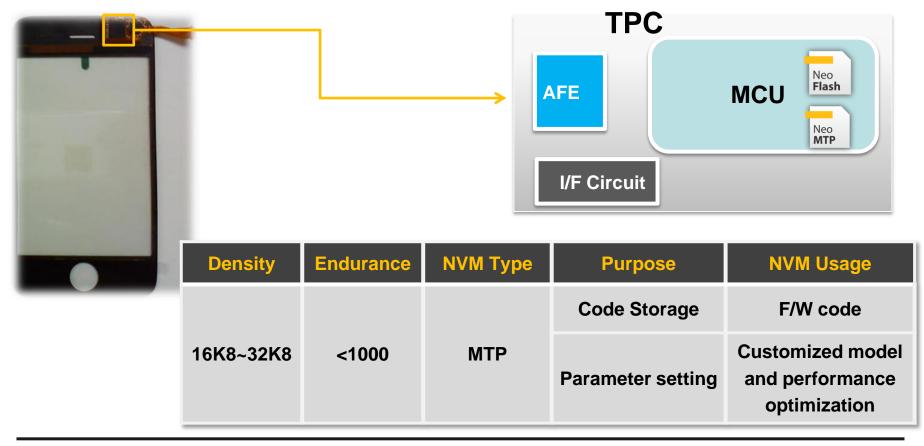
Application Processor	Density	NVM Type	Purpose	NVM Usage
	2Kb~4Kb	ОТР	Trimming	DC/DC, Bandgap
			Parameter Setting	Design flexibility & Performance optimization
			Code Storage	Start-up behavior & smart power saving algorithm
Base Band IC	PMIC	Neo Bit		

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Touch Panel Controller ICs

Process Technology : 0.16um HV/0.11um G

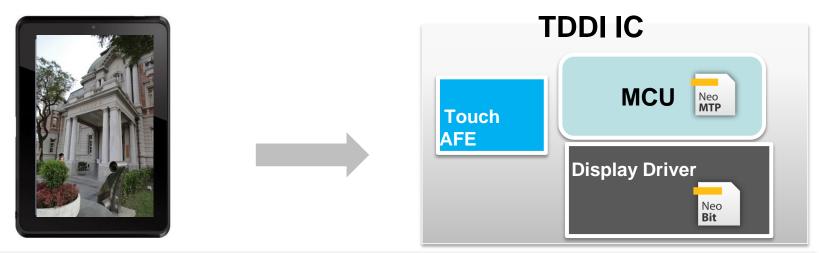


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In-Cell Touch Panel Controllers ICs

Process Technology : 0.11um HV/80nm HV/55nm HV



Density	Endurance	NVM Type	Purpose	NVM Usage
2K8~4K8		ОТР	Trimming	Accuracy
200~400			Code Storage	Gamma Table
	6K8~32K8 <1000 MTP		Code Storage	Touch F/W Code
16K8~32K8		МТР	Parameter setting	Performance Optimization

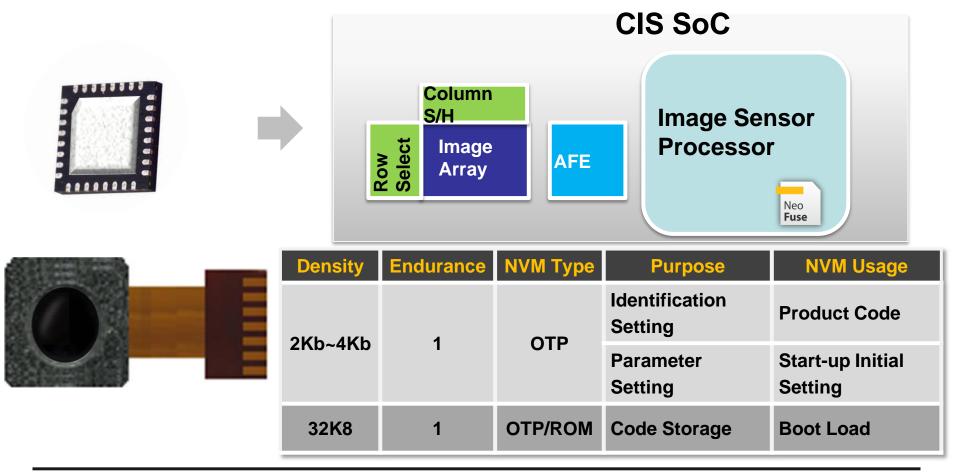
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CMOS Image Sensor

Process Technology : 0.11um CIS/90nm CIS/65nm CIS

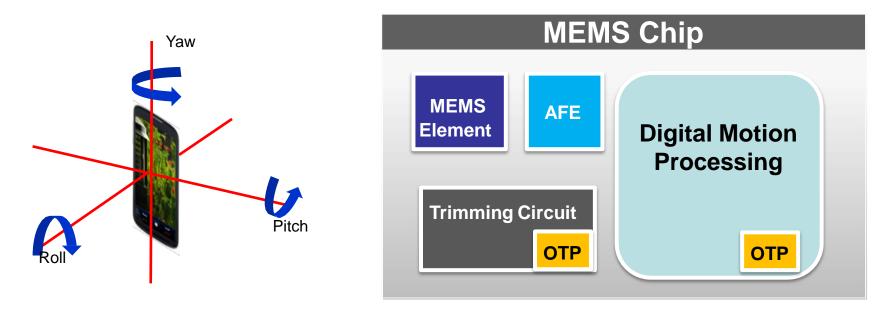


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MEMS 180/160/15x nm HV/Logic for MEMS Controller



Density	NVM Type	Purpose	NVM Usage
2Kb~4Kb	Kb OTP	Trimming	Factory trimming
		Parameter Setting	Signal filtering
	Code Storage	Geometric computation	

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Replacement of Embedded Flash for Competitiveness Improvement

product design & manufacturing by embedded Flash Logic Process + 10 Masks

30% more cost reduction

wafer cost & testing time

product design & manufacturing by Embedded Logic NVM (OTP/MTP) Logic Process

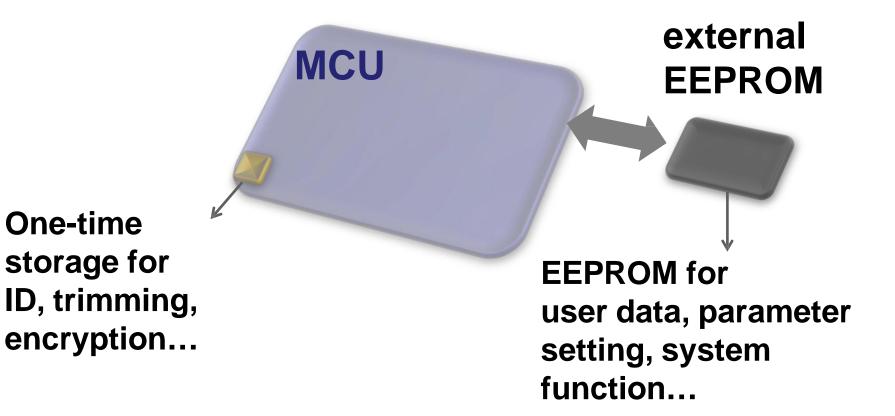
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MCU

MCU

MCU Applications with EEPROM



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One-time



NeoBit + NeoEE

Hybrid NVM solution (NeoBit + NeoEE) with customized SPEC & optimized size



One single IP by integration of NeoBit & NeoEE Help for system size reduction

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Wafer Demand by IC Type

Equa to 8-inch wafer (K)
5740
5255
2945
2683
2500
2215
1955
708
619
602
463
348
239
231
166
140
126
120
107
104
90
88
82
67
47
38
23
16
14
3
3
0

2015 Q3 updated

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Prospect for the future

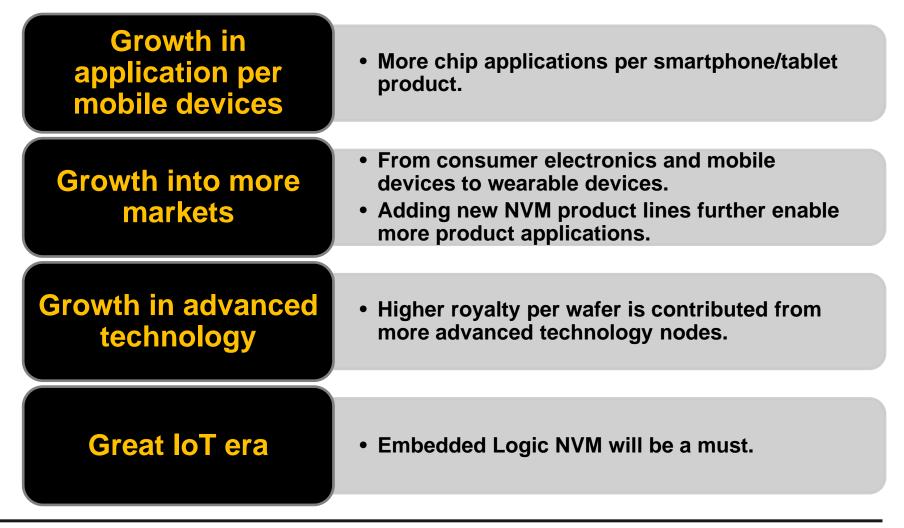
- License fee expected to grow due to the successful development in advanced nodes.
- PMIC continually extends to the application of wireless charger and fast charger related products.
- 55nm DDI continues volume production. More than 50 tape out were done in past two years.
- 28nm Set-top Box processor starts to volume production. There are more customers will tape out new products in Q1 2016.



Prospect for the future

- Fingerprint and CIS customers start to small volume production.
- The qualification of 16nm FF⁺ started and expected to be completed at end of March 2016.
- 16nm FFC verification is successful. Qualification will be started in Q1 2016.
- 10nm FF IP will tape out in March and already has customer engagement.
- More projects on automotive, the applications extend from PMIC to LCD Driver.

Key Growth Drivers





Q & A



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