ememory

A Leading Logic NVM Company

IPR Notice

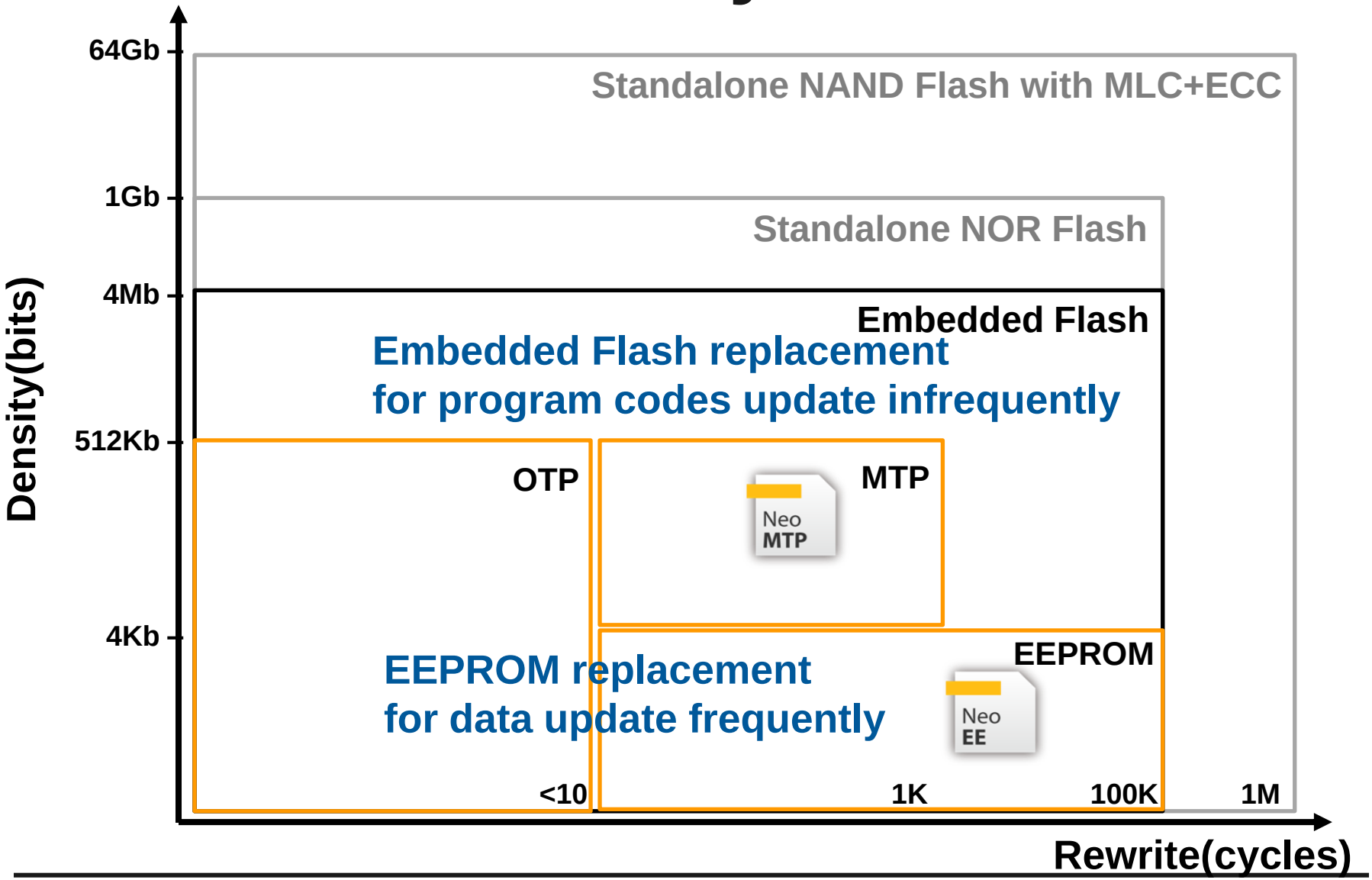
Cautionary Statement

This presentation contains forward-looking statements, which are subject to risk factors associated with semiconductor and intellectual property business. It is believed that the expectations reflected in these statements are reasonable. But they may be affected by a variety of variables, many of which are beyond our control. These variables could cause actual results or trends to differ materially and include, but are not limited to : wafer price fluctuation, actual demand, rapid technology change, delays or failures of customers' tape outs into wafer production, our ability to negotiate, monitor and enforce agreements for the determination and payment of royalties, any bug or fault in our technology which leads to significant damage to our technology and reputation, actual or potential litigation, semiconductor industry cycle and general economic conditions. Except as required by law, eMemory undertakes no obligation to update or revise any forward-looking statements, whether as a result of new information, future events, or otherwise.

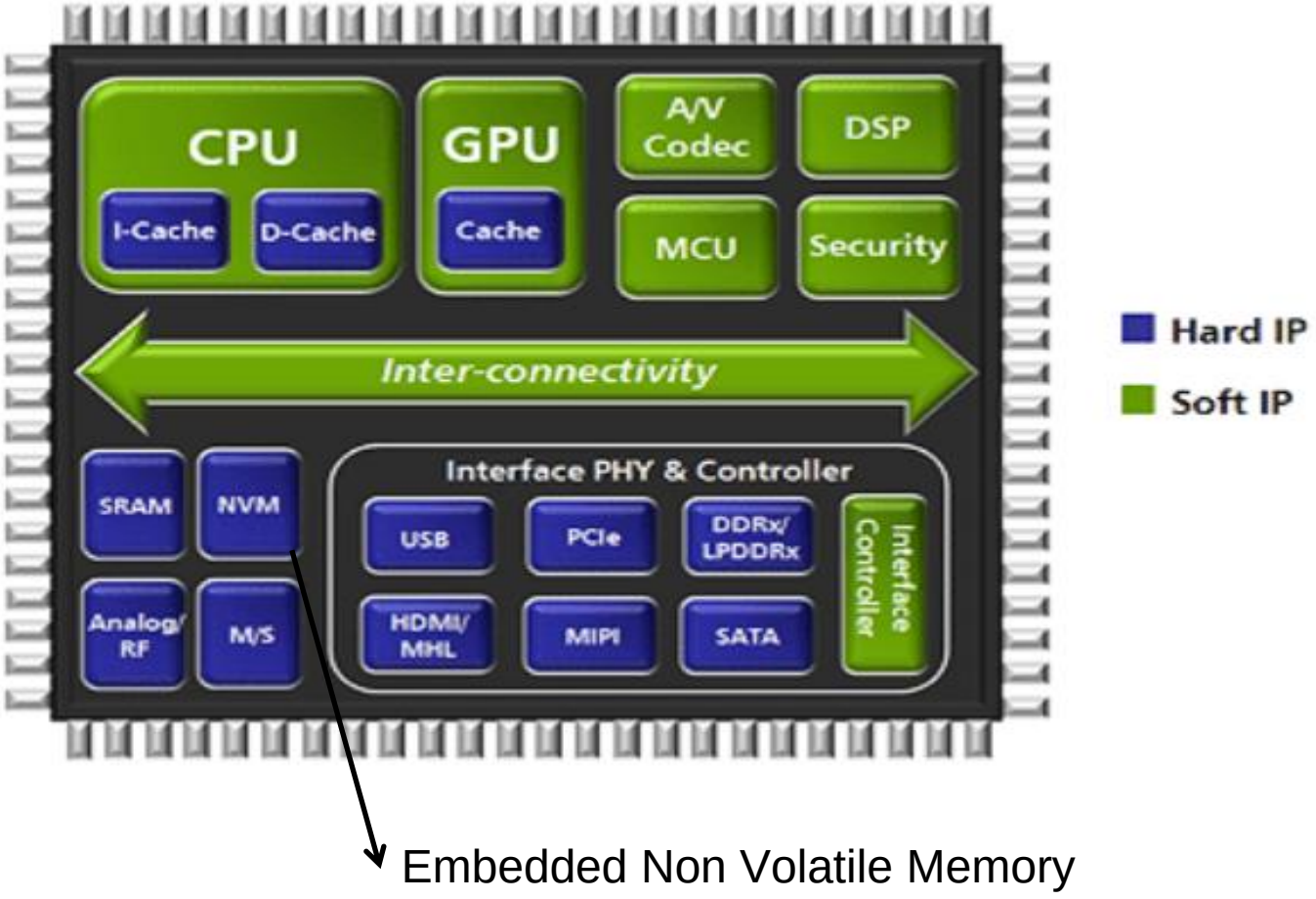
Outline

- **Business Model**
- **Review of Operations**
- **Growth Opportunity and Future Outlook**
- **Q & A**

Nonvolatile Memory Classifications



SOC Block Diagram



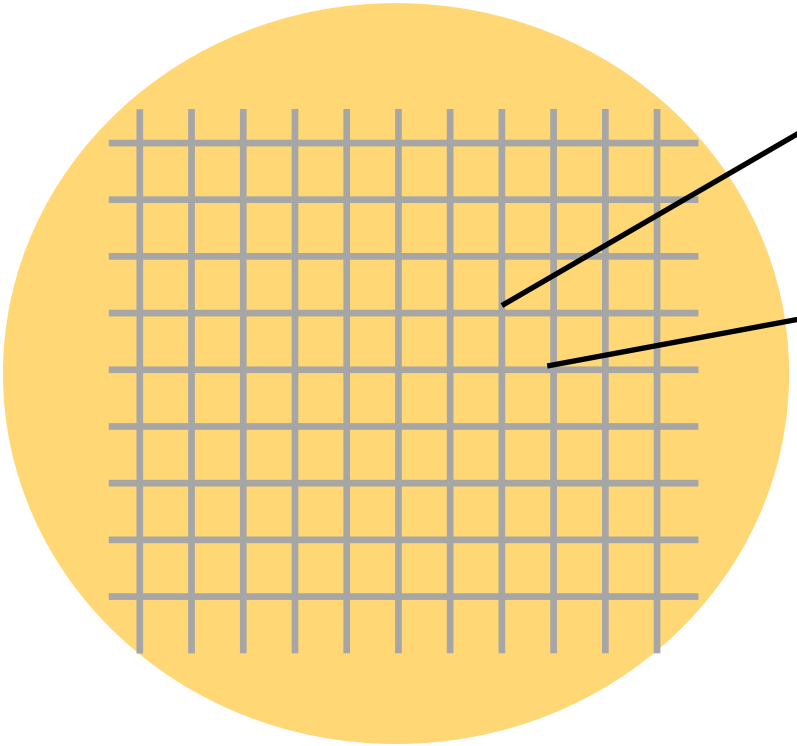
Source : tsmc

Embedded NVM Technologies

	ROM	eFuse (OTP)	Antifuse (OTP)	CMOS Floating Gate (OTP)	CMOS Floating Gate (MTP)	Embedded Flash
Cell Structure	Transistor	Poly Fuse	Antifuse	Floating Gate	Floating Gate	Floating Gate
Standard CMOS Compatible	Yes	Yes	Yes	Yes	Yes	No
Bitcell Area	< 1	50	1	2	4	1
Endurance	No	No	< 10	< 10	10K-100K	100-1000K
Density	4Kb-1Mb	256bit-4Kb	16bit-1Mb	16Kb-1Mb	1Kb-2M	64Kb-4Mb
Security	Low	Low	High	High	High	High
Additional Steps	None	None	None	None	None	+10 Mask

- ROM not programmable, eFuse cannot scale beyond 16Kb, embedded flash expensive and cannot scale after 40 nm
- eMemory's IPs: OTP (antifuse, floating gate) and MTP (floating gate)

Considerations for IP Adoption



Customer Product

IP

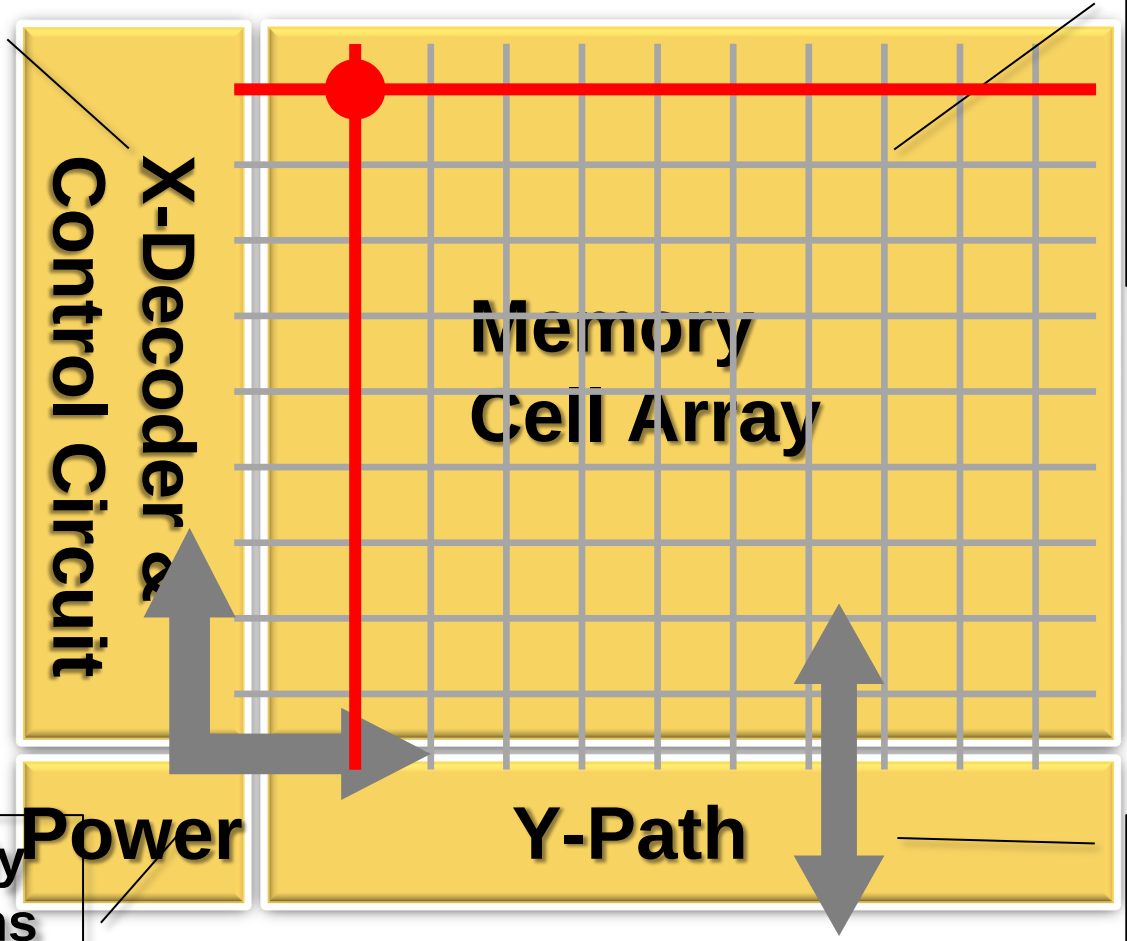
Generally,
IP size is less than 10% of product size

Customers Request

1. **100% IP Reliability**
2. **No Mask Adder**
3. **Low Testing Cost**
4. **On call Service**
5. **Acceptable IP Size**

Inside Nonvolatile Memory IP

Program, Erase and Read operation control



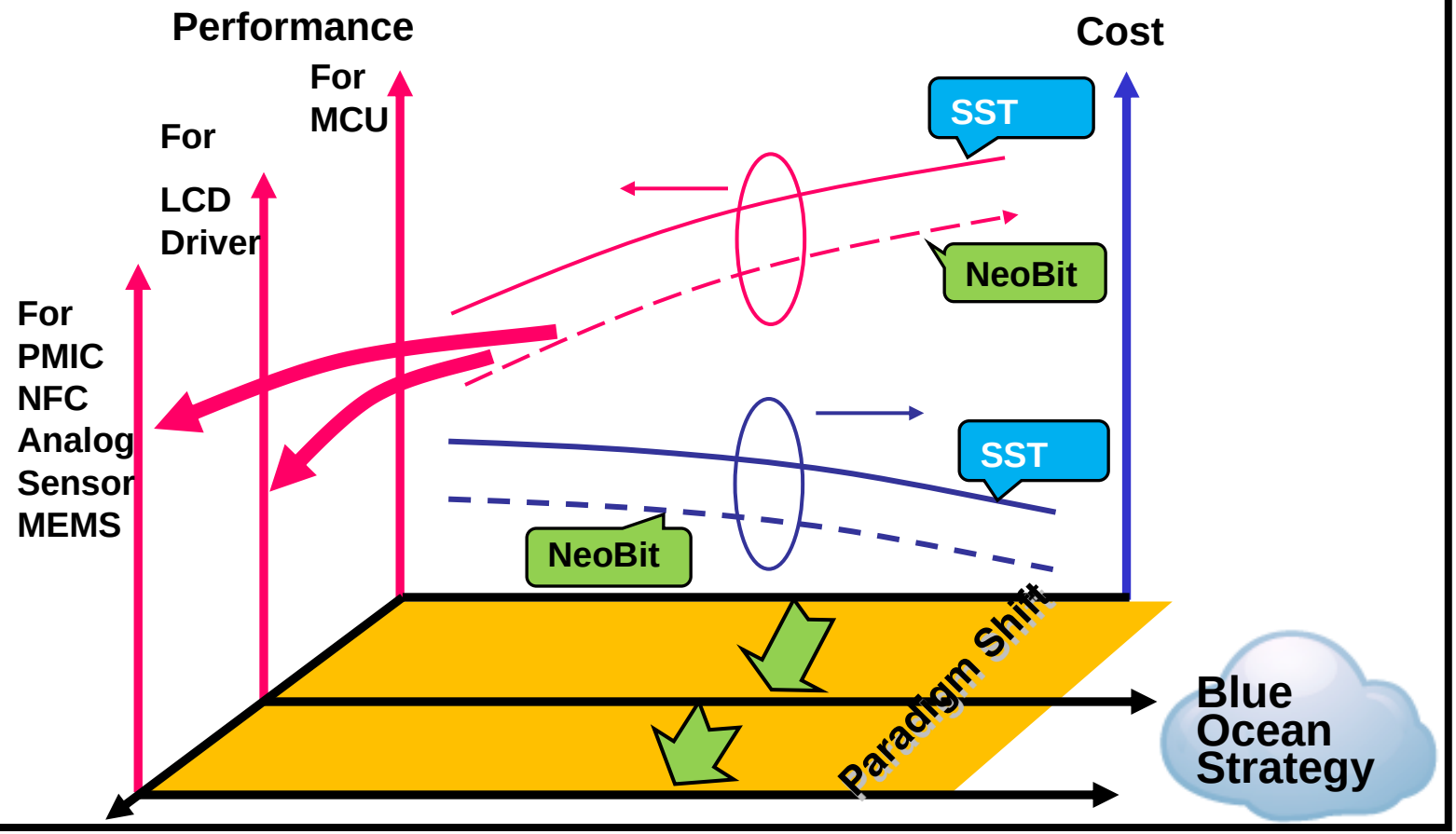
Where data is stored. Each cross point has a memory cell.

Power supply for operations

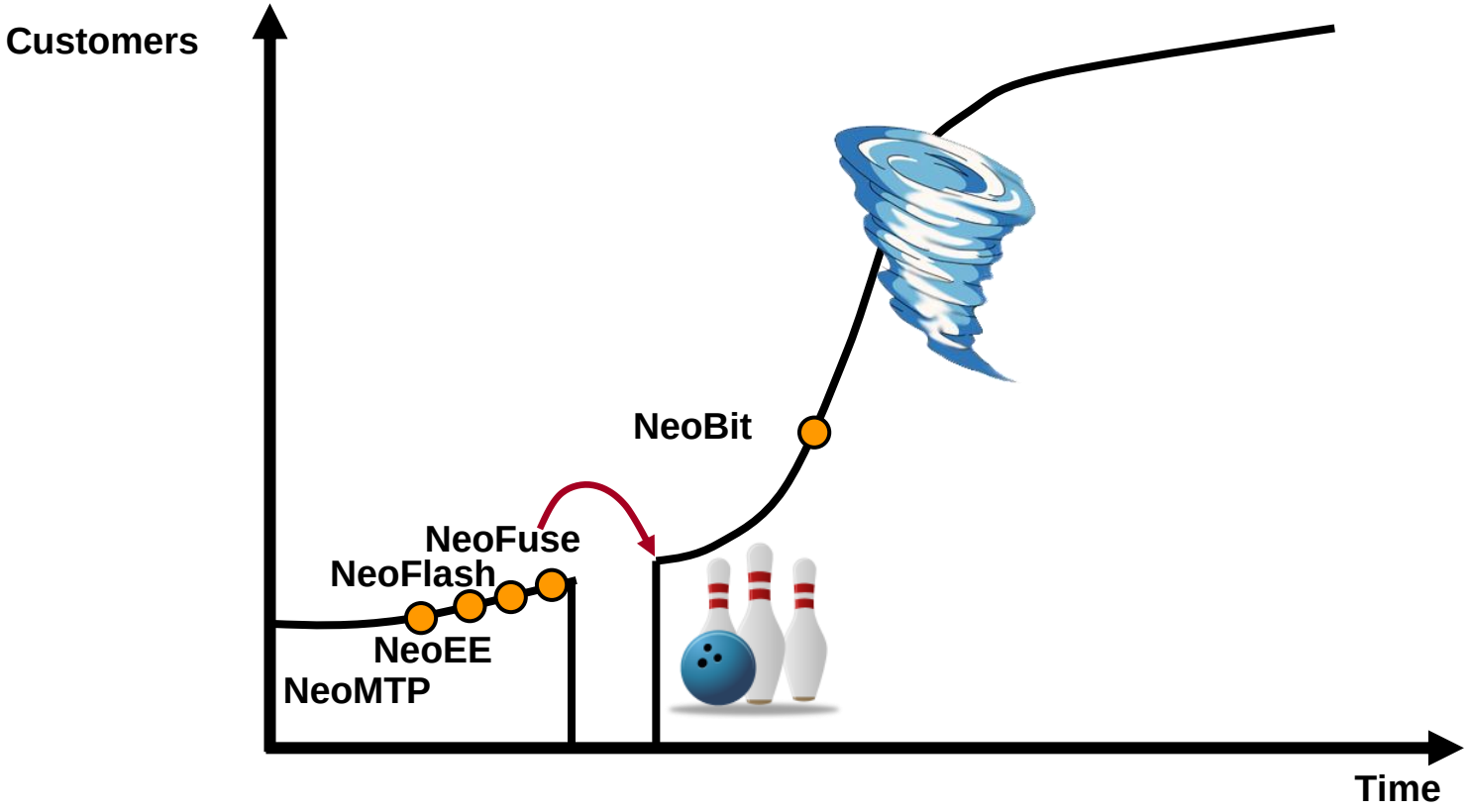
Data input & output

What We Have Done

- *Innovation, Innovation, and Innovation !*

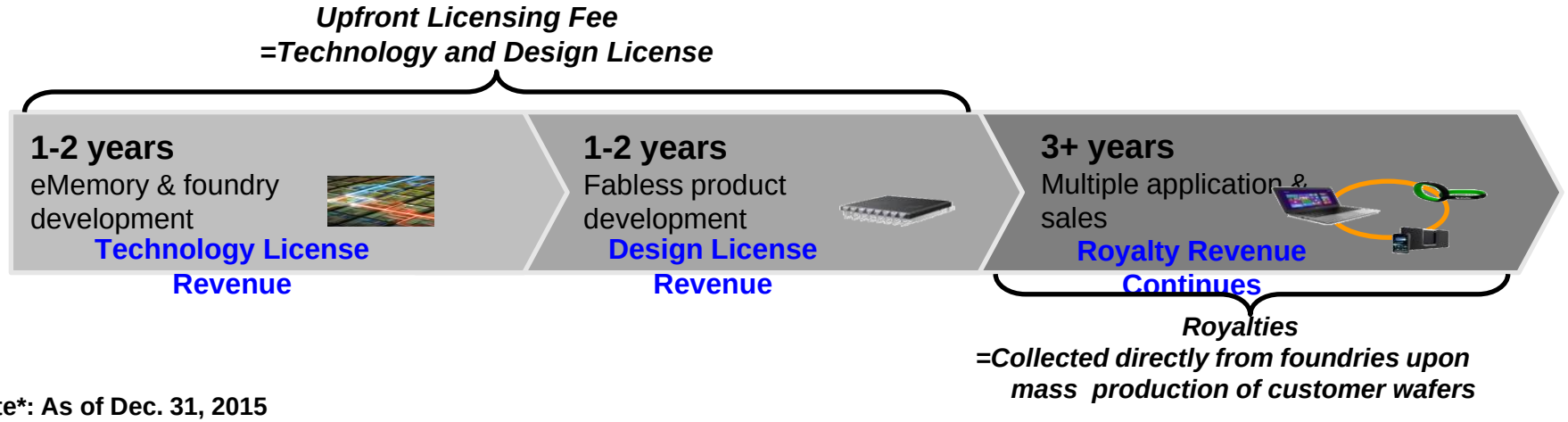


Crossing the Chasm



Business Model

- **Founded in 2000. First customer engaged in 2002. Achieved profitability in 2005 and IPO in 2011. The largest logic non-volatile memory IP company, 228 employees (157 R&D)*.**
- **Since its IPO, the company initiated no new fund raising or bank debt, and has distributed in excess of 100% of earnings in cash dividends.**
- **Growth Indices: 1) No. of on-going technology platforms**
  2) No. of design licenses
  3) Royalty



Note*: As of Dec. 31, 2015

Worldwide Customers

	Taiwan	China	Korea	Japan	North America	Europe	Others
Foundry	5	7	3	2	1	1	1
IDM	0	0	0	8	2	1	0
Fabless	237	351	51	36	181	94	40

Foundry

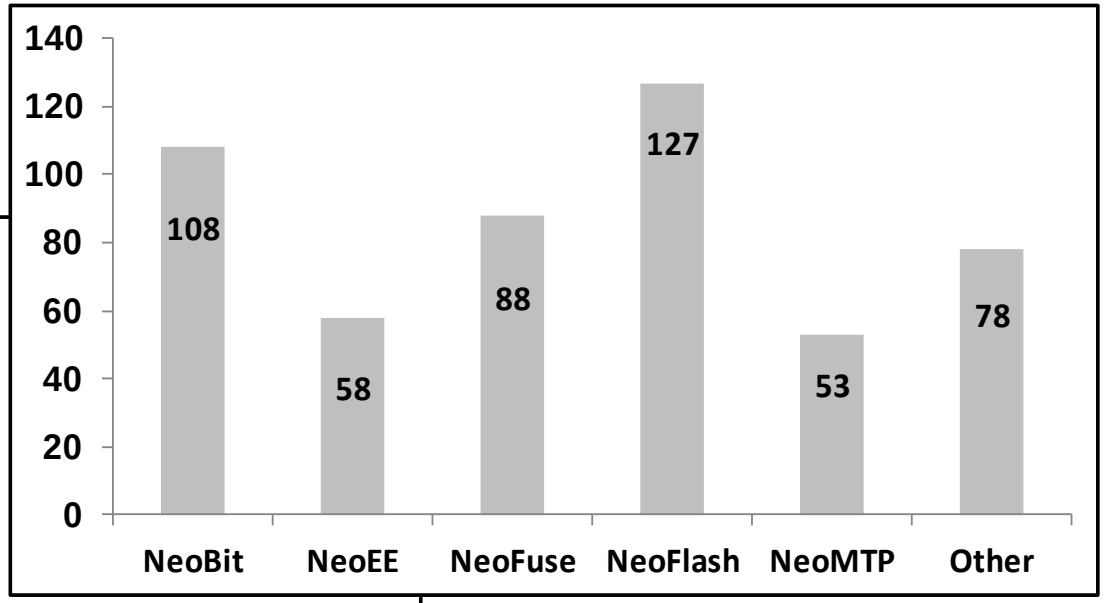
tsmc, UMC, VIS, SILTERRA, HS 华虹宏力, GLOBALFOUNDRIES, SMIC, MagnaChip, Maxchip 鉅晶電子, ROHM SEMICONDUCTOR, SK hynix, Dongbu HiTek, HEJIAN, FUJITSU, Powerchip 力晶科技, CSMC A LEADING ANALOG FOUNDRY, HLMC, asmc Advanced Semiconductor Manufacturing Corporation Limited, Altis

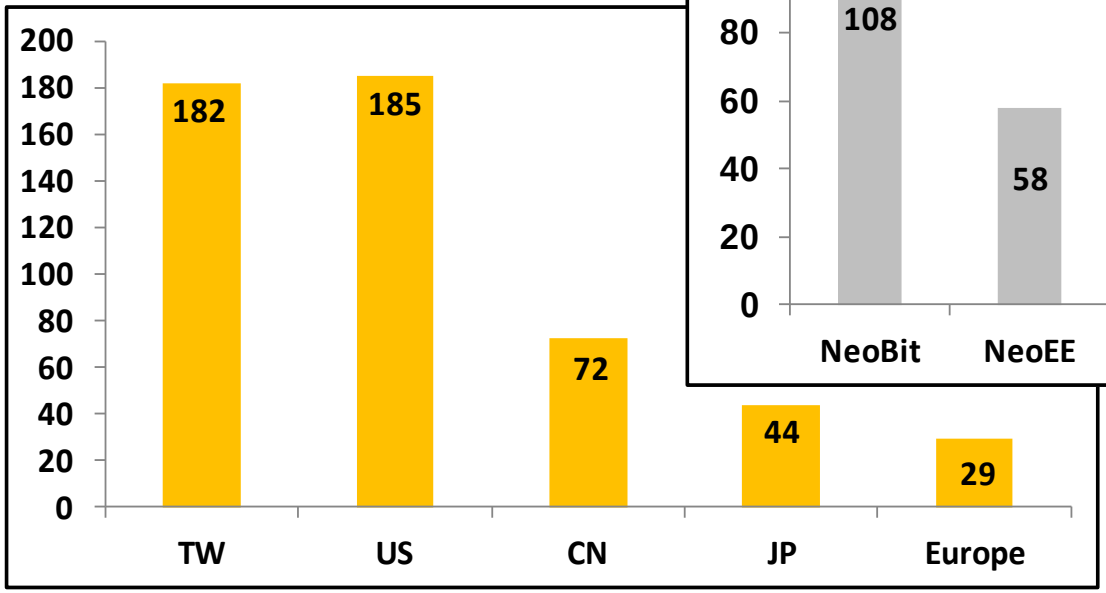
IDM

FUJITSU, OKI, MITSUMI, MITSUBISHI ELECTRIC Changes for the Better, JRC, MAXIM, RICOH, RENESAS, SII, TOSHIBA, ON Semiconductor, ON, NXP

Patent Portfolio

	Q3 15	Q4 15	Diff.
Pending	187	187	-
Issued	304	325	+21
Total	**491**	**512**	**+21**

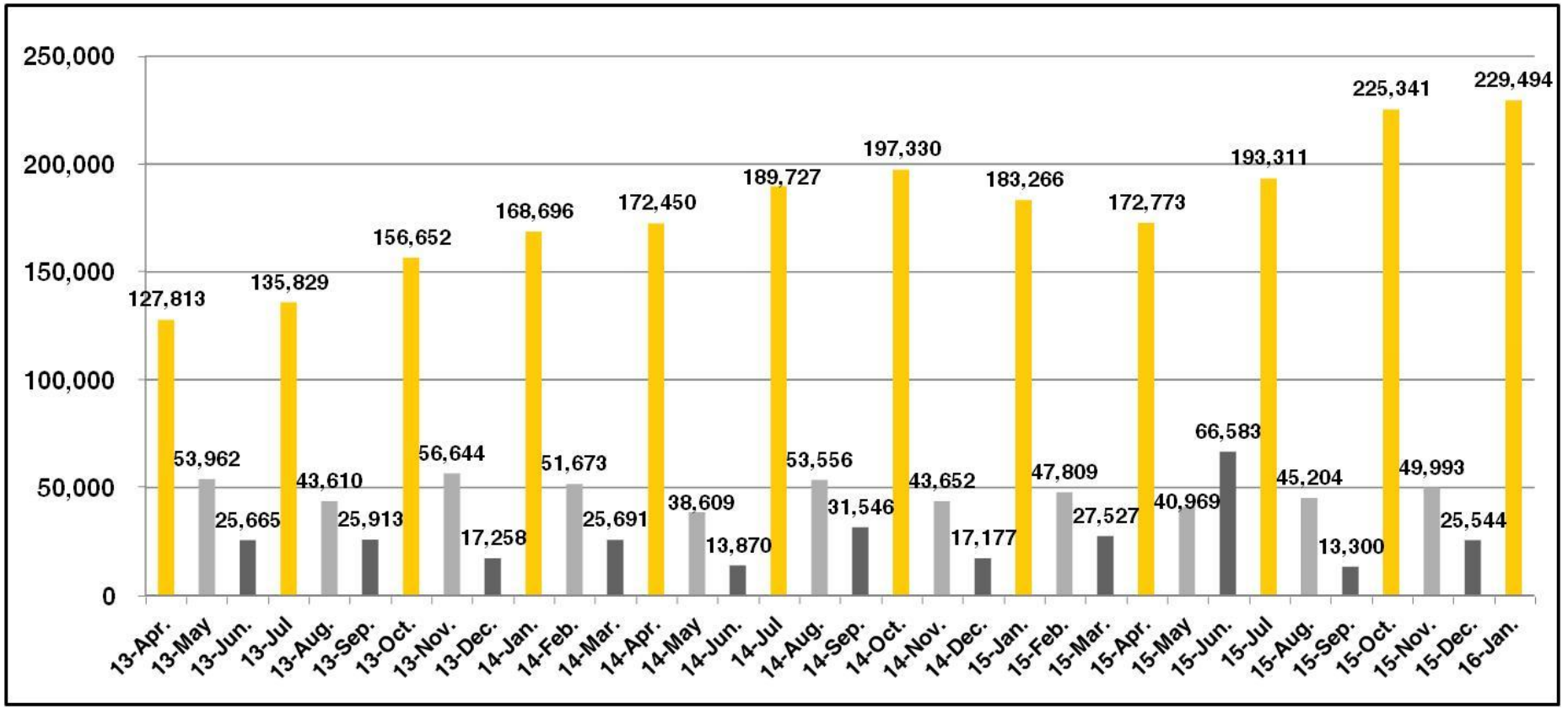




Quarterly Revenue Pattern

- **The quarterly royalty from most of foundries are collected at first month of each quarter and from some other foundries are collected at second month, and none at third month.**

Unit：NTD Thousands



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Q4 Revenue Breakdown

Unit: NTD thousands

	2015 Q4	2015 Q3	QoQ	2014 Q4	YoY	2015	2014	YoY
Licensing	69,307	38,167	81.59%	51,849	33.67%	267,512	246,073	8.71%
Royalty	231,571	213,648	8.39%	206,310	12.24%	824,108	757,904	8.74%
Total	300,878	251,815	19.48%	258,159	16.55%	1,091,620	1,003,977	8.73%

Unit: Number of contracts

		2015 Q4	2015 Q3	2015	2014
Technology Licenses		11	4	28	21
Design Licenses	NRE	9	10	57	82
	Usage	104	76	349	363

Financial Income Statement

(Unit: NTD thousands)	Q4 15	Q4 14	% change	2015	2014	% change
Revenue	300,878 *	258,159	16.5%	1,091,620 *	1,003,977	8.7%
Gross Margin	100% *	100%	-	100% *	100%	-
Operating Expenses	156,216 *	148,466	5.2%	570,403 *	540,286	5.6%
Operating Margin	48.1% *	42.5%	+5.6ppts	47.7% *	46.2%	+1.5ppts
Net Income	128,090 *	100,931	26.9%	479,111 *	418,604	14.5%
Net Margin	42.6% *	39.1%	+3.5ppts	43.9% *	41.7%	+2.2ppts
EPS (Unit: NTD)	1.69 *	1.33	27.1%	6.32 *	5.52	14.5%
ROE	28.4% *	23.4%	+5.0ppts	26.6% *	24.3%	+2.3ppts

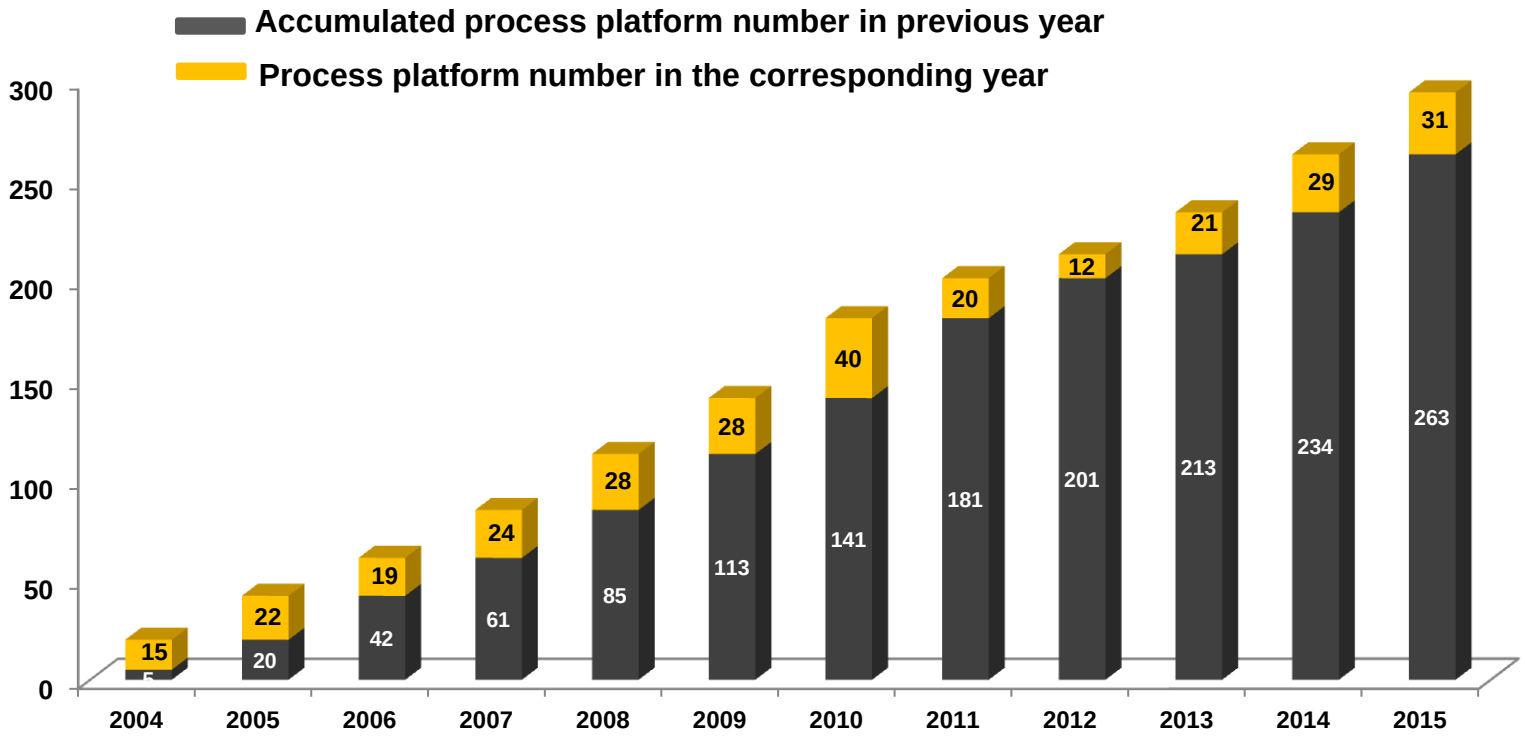
* Unaudited

Technology License

Unit: Number of contract

Year	2013	2014	2015
License number	19	21	28

Note: The terms (including number of process platforms and licensing fees) for each technology license are set contractually. Payments are made according to set milestones, and there are no particular seasonal factors involved.



Current Technology Development Platforms

- Total (As of Dec.) : 100
- 16 for NeoBit, 38 for NeoFuse, 26 for NeoEE, and 20 for NeoMTP.

	10nm	14/16nm	28nm	40nm	55/65nm	80/90nm	0.11~ 0.13um	0.15~ 0.18um	>0.25 um	Total
NeoBit	-	-	-	-	-	-	5	11	-	16
NeoFuse	1	3	9	4	9	3	6	3	-	38
NeoFlash	-	-	-	-	-	-	-	-	-	0
NeoEE	-	-	-	2	-	1	6	17	-	26
NeoMTP	-	-	-	1	2	2	4	11	-	20

Current Technology Development Platforms

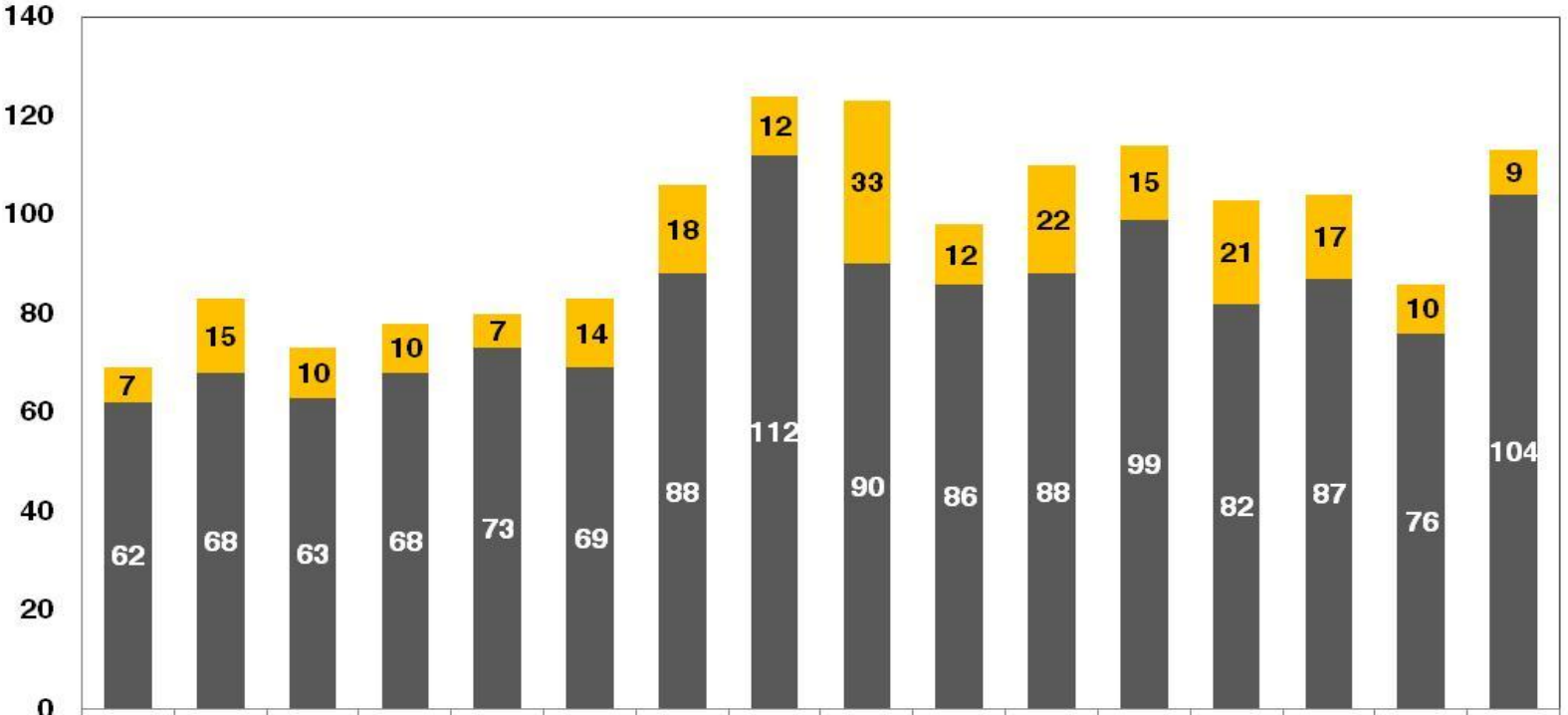
12" Fabs	Production	Development	NVM Type	Process Type
10nm	0	1	OTP	FF
14/16nm	0	3	OTP	FF+
28nm	5	9	OTP	LP/HPM, HLP/HPM, LPS
40nm	2	7	OTP, MTP	HV-DDI, LP
55/65nm	10	11	OTP, MTP, Flash	LP, HV-DDI, HV-OLED, DRAM, CIS
80/90nm	5	6	OTP, MTP	HV-DDI, HV-OLED, LP
0.13/0.11um	6	4	OTP, Flash	HV-DDI, BCD, Generic
0.18um	1	0	OTP	BCD

8" Fabs	Development	NVM Type	Process Type
0.13/0.11um	17	OTP, MTP, Flash	HV-DDI, BCD, LP, RF, CIS, LL
0.18/0.16/0.152um	42	OTP, MTP	Generic, LP, LL, MR, HV, Green, BCD
0.25um	0	OTP, MTP	BCD
0.35um	0	OTP	UHV

*As of Dec. 31, 2015

Quarterly Design Licensing (New Tape Out)

- *Total 406 NTO in 2015 (445@2014 393@2013, 303@2012, 258@2011)*

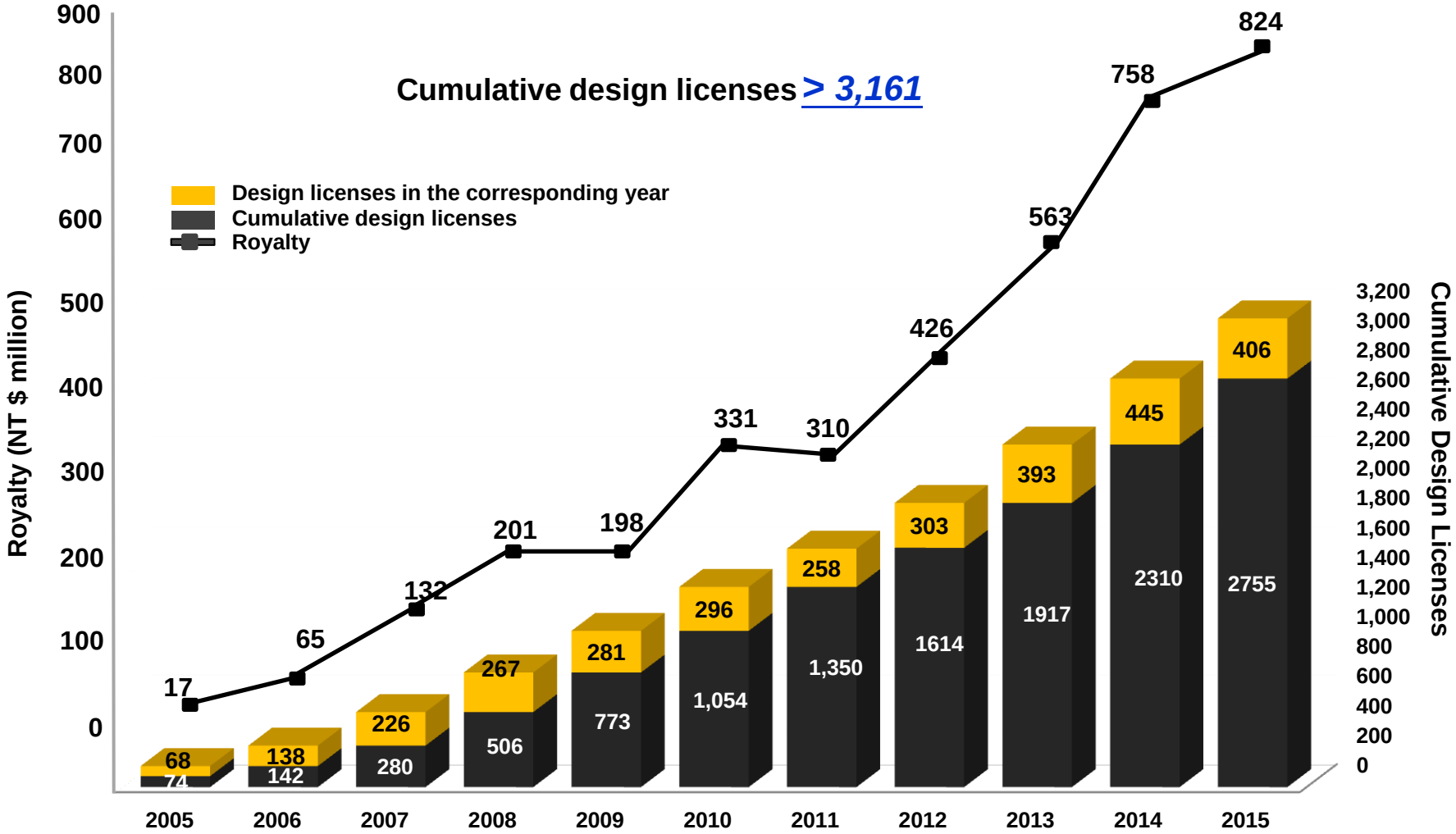


	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
	2012				2013				2014				2015			
NRE	7	15	10	10	7	14	18	12	33	12	22	15	21	17	10	9
Usage	62	68	63	68	73	69	88	112	90	86	88	99	82	87	76	104

Usage：Usage of pre-qualified and verified IP (charged by per product tape out or annual package), the cycle time from design implementation to royalty payments for mass production is faster, typically less than one year.

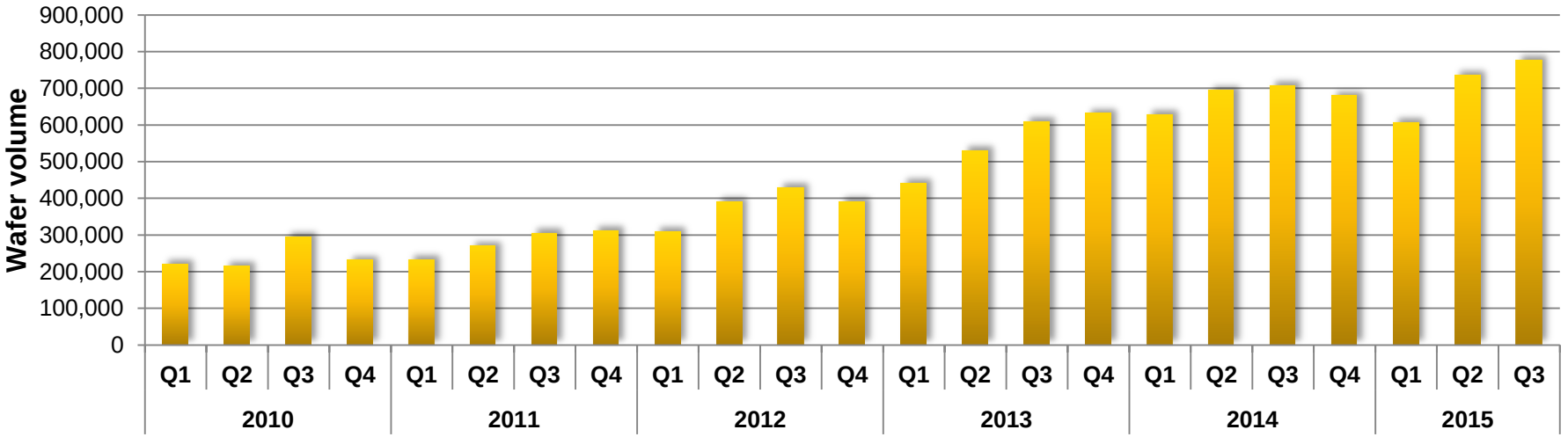
NRE: NRE covers the customization of IP that must undergo new verification or qualification. It typically requires 1 to 1.5 years before resulting in royalty revenue.

Cumulative Licenses Drive Future Royalties



note 1: Due to the 2009 recession, royalty income was down annually 1.5%.
note 2: Pre-payment of royalty fees by a single customer contributed to 2010 annual growth of 67%, causing a drop of 6.3% in the following year, 2011.
note 3: CAGR for 2009-2013 was 30%.

Wafer Production Volume



embedded eMemory IP in T Company ($revenue); * % of Process node in T company total revenue in Q4 15

	Process node	*% of T	Q4 15	Q3 15	2015	2014
8”	0.25/0.35	4%	47.61%	38.2%	33.49%	30.5%
	0.15/0.18	11%	10.11%	7.9%	8.73%	11.9%
	0.11/0.13	3%	29.24%	30.9%	29%	20.8%
12”	90nm	7%	20.20%	21.8%	19.85%	16.3%
	65nm	11%	0.61%	0.9%	0.55%	0%
	40/45nm	14%	0%	0%	0%	0%
	28nm	25%	0.18%	0.02%	0.05%	0%
	16/20nm	24%	0%	0%	0%	0%
8”		19%	21.64%	16.3%	16.64%	15.6%
12”		81%	1.88%	2.3%	1.87%	1.4%
Total		100%	5.42%	5.0%	4.76%	4.5%

Outline

- Business Model
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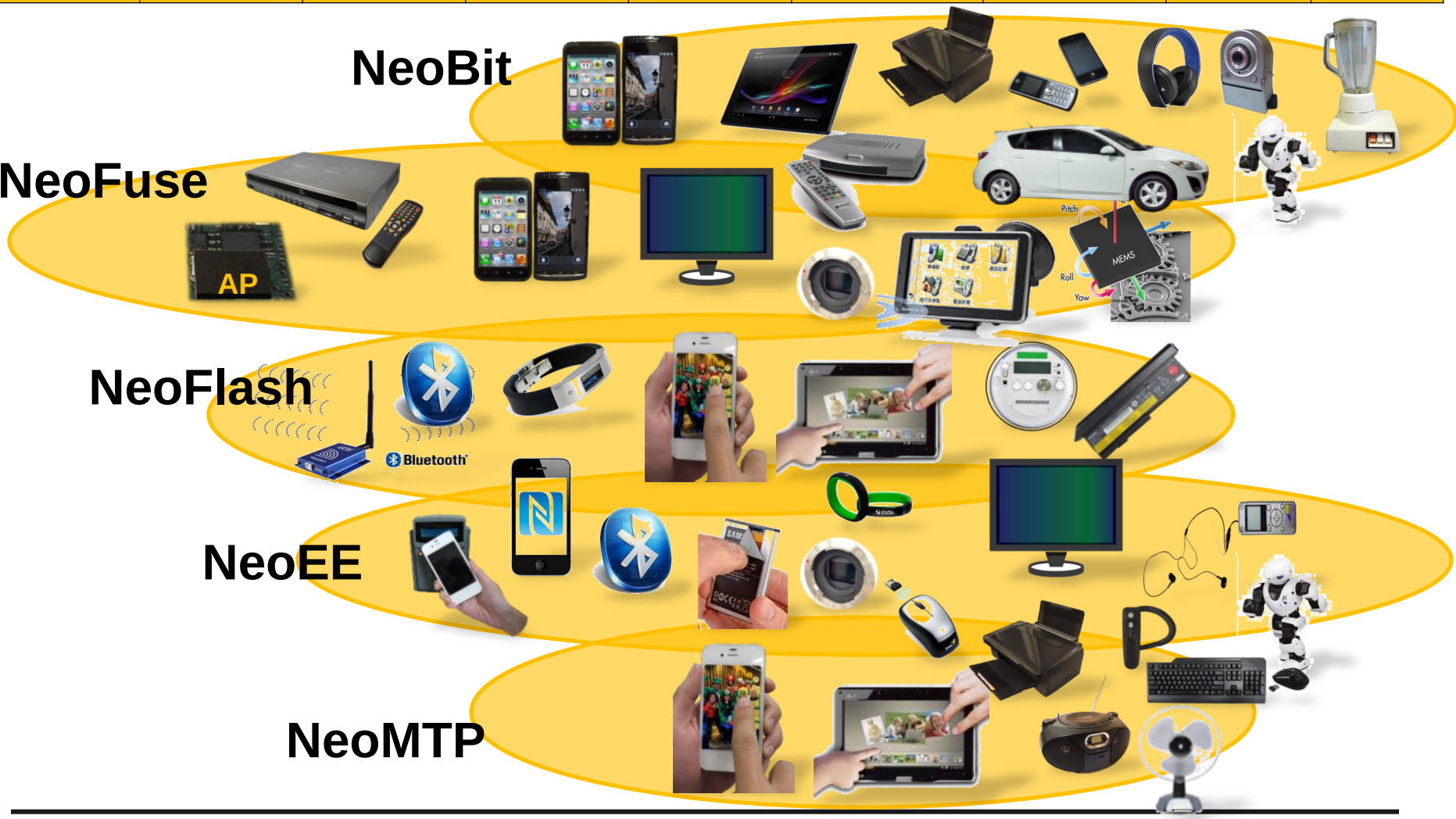
eMemory's NVM Technologies

- **Logic NVM portfolio offers one-stop-shop solution.**
  - Compatible to any process
  - Robust structure
  - Low process cost
  - Competitive macro sizes
  - Easy integration
  - Easy porting

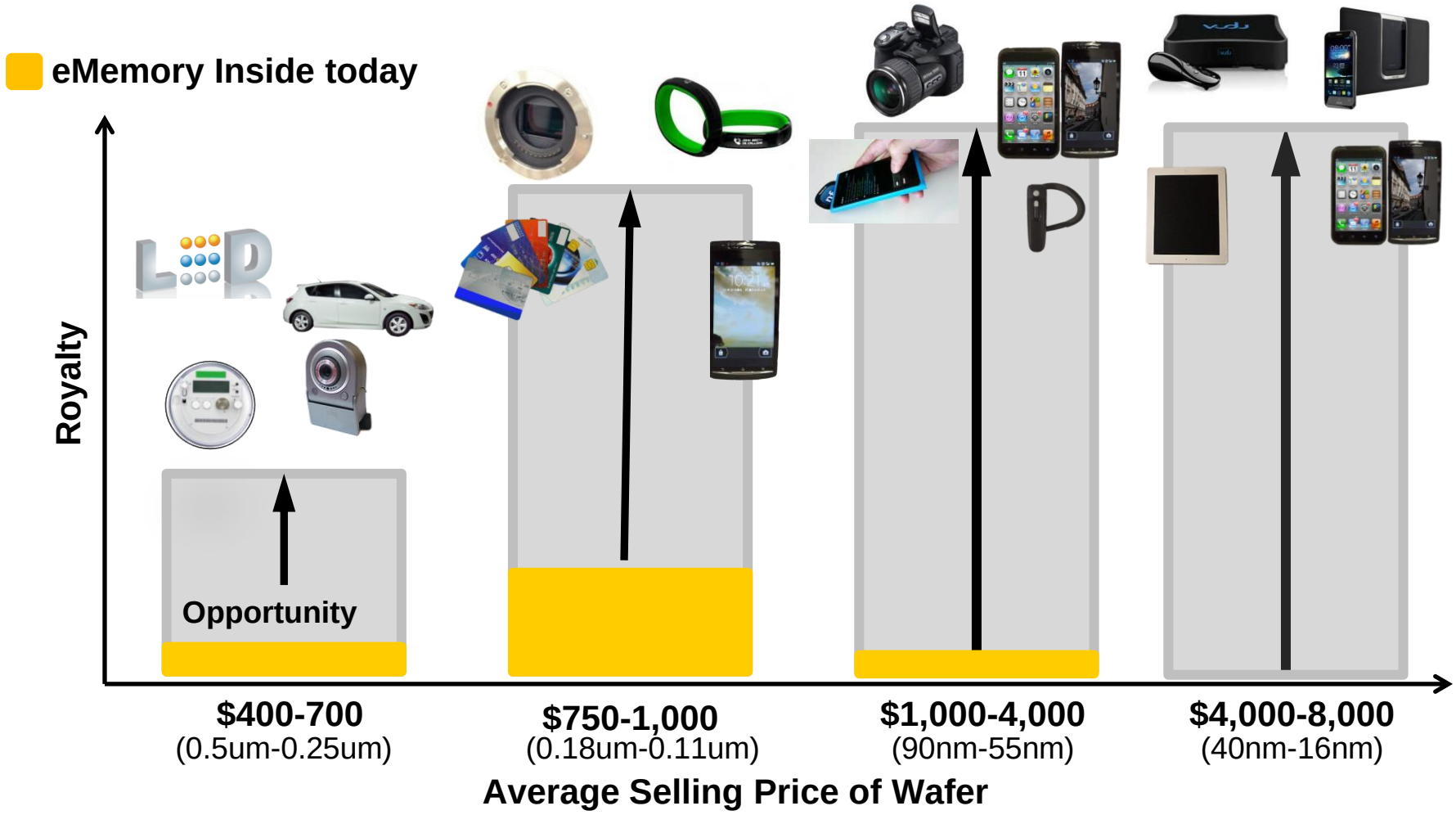
eMemory's NVM Technology	OTP		MTP		
	NeoBit	NeoFuse	NeoFlash	NeoEE	NeoMTP
Product Type	OTP	OTP	Flash	EEPROM	MTP
Endurance (Cycles)	10	10	1K~10K	10K~100K	1K~10K
Additional Mask Steps	0	0	2-3	0	0
Technology	Floating gate	Anti-Fuse	SONOS	Floating gate	Floating gate
Scalability	Simple	Simple	Simple	Simple	Simple
Memory Density	HD < 512Kb GHD < 16Mb	< 4Mb	< 2Mb	< 4Kb	< 512Kb

Applications by Technology

12"						8"		
16/20nm	28nm	40nm	55/65nm	80/90nm	110/130nm	160/180nm	250nm	350nm

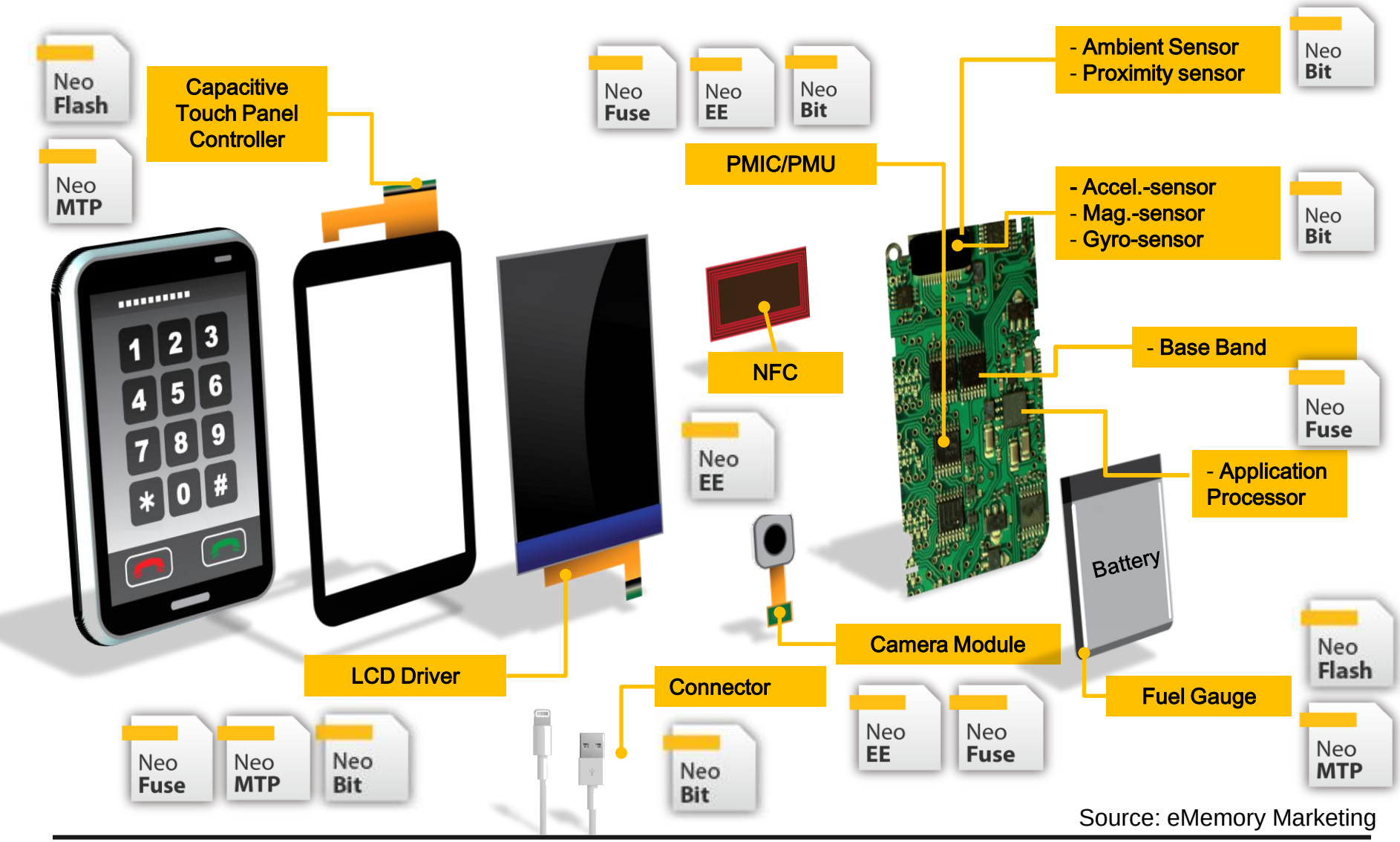


Opportunity at all Price Points



Note: 2.2 million 8" equivalent wafers with eMemory IP were shipped in 2013. (~5% of WW foundry shipment)

eMemory IP in Smart Phone



Source: eMemory Marketing

Benefits from Using eMemory IPs

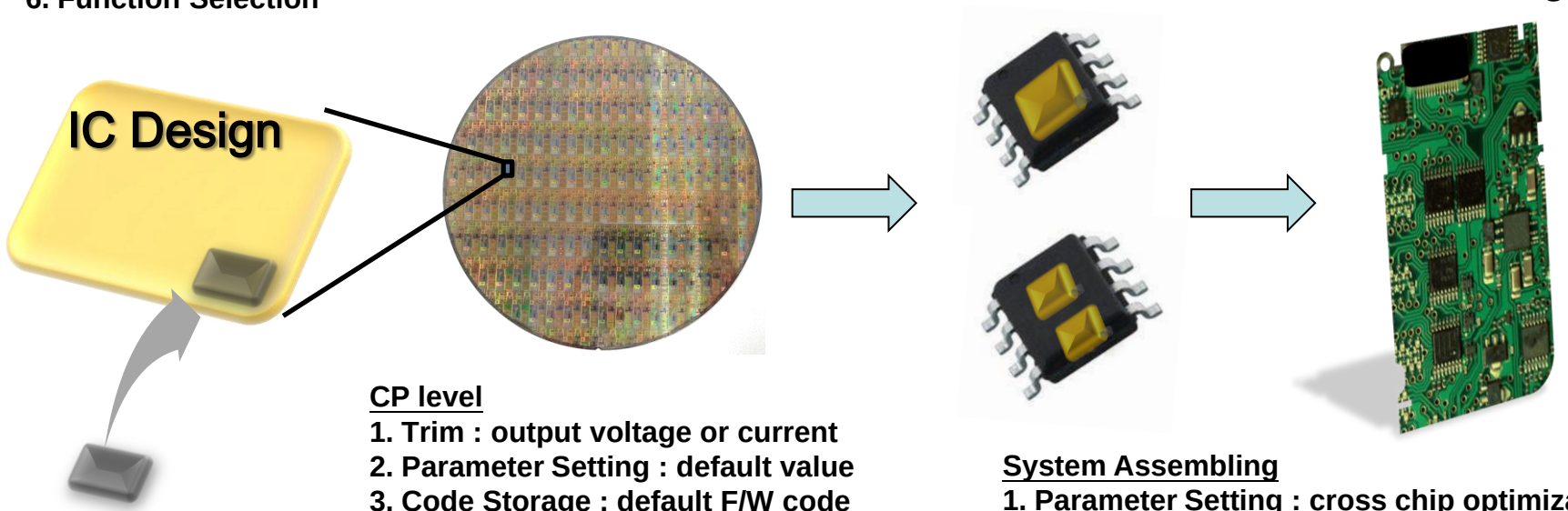
Design-in for
1. Trimming
2. Parameter Setting
3. Code Storage
4. Identification Setting
5. Encryption
6. Function Selection

Package/FT level
1. Trim : SPEC shift
2. Parameter Setting : cross chip optimization
3. Identification Setting : manufacturer resume
4. Function Selection : setting for target market

CP Test

Package/FT

System Assembling



CP level
1. Trim : output voltage or current
2. Parameter Setting : default value
3. Code Storage : default F/W code

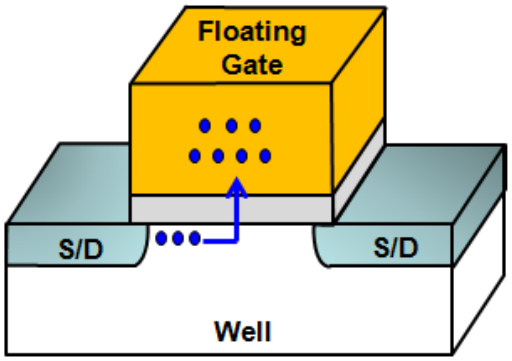
System Assembling
1. Parameter Setting : cross chip optimization
2. Code Storage : F/W code modification
3. Identification Setting : manufacturer resume
4. Encryption : Security algorithm or key storage

Invisibility for Security

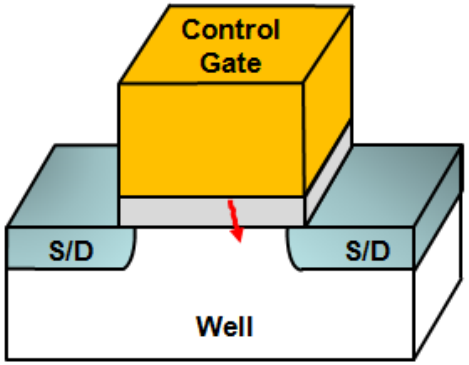
- Provide “Invisible Hardware Key” for invisible storage
- Prevent reverse-engineering to detect content of security key
- Protect firmware and hardware of ICs from pirating
- Extend & protect customer’s business

eFuse Key: Data is easily observed

Invisible Hardware Key : Data is hard to be detected



Floating Gate



Anti-Fuse

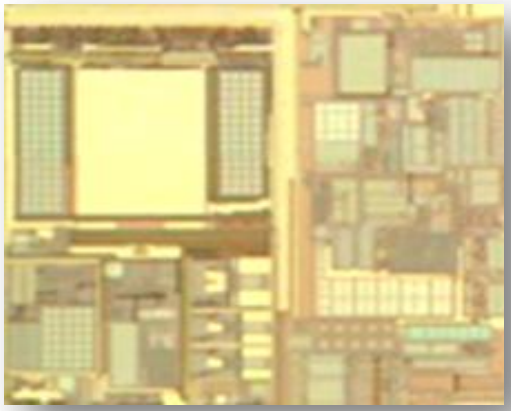
Security & Protection

Authorized Product

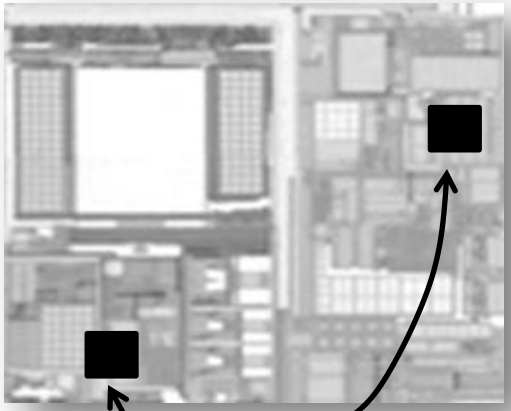
Fake Product

reverse copy

re-produce

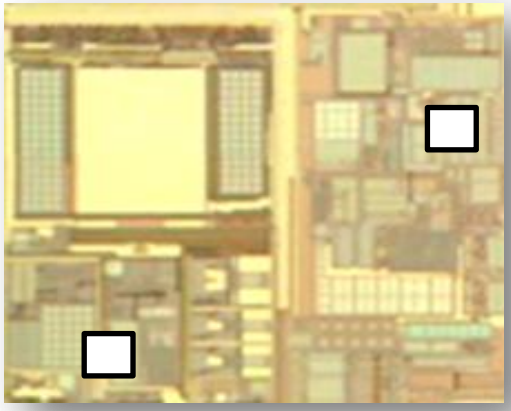


without protection



reverse copy

re-produce

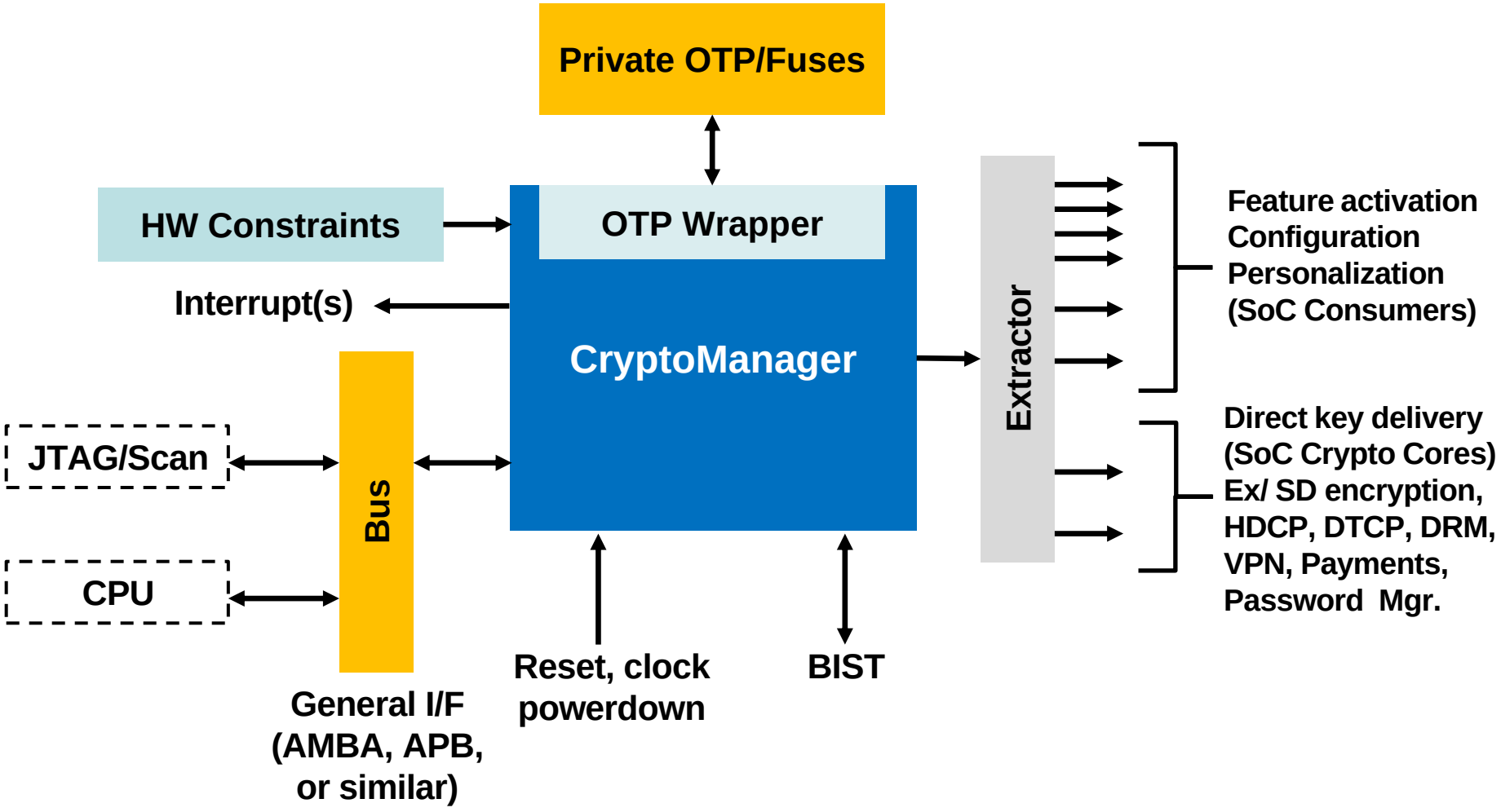


with protection

Security IP/Code by Authorized Use

Can NOT Work w/o Security IP/Code

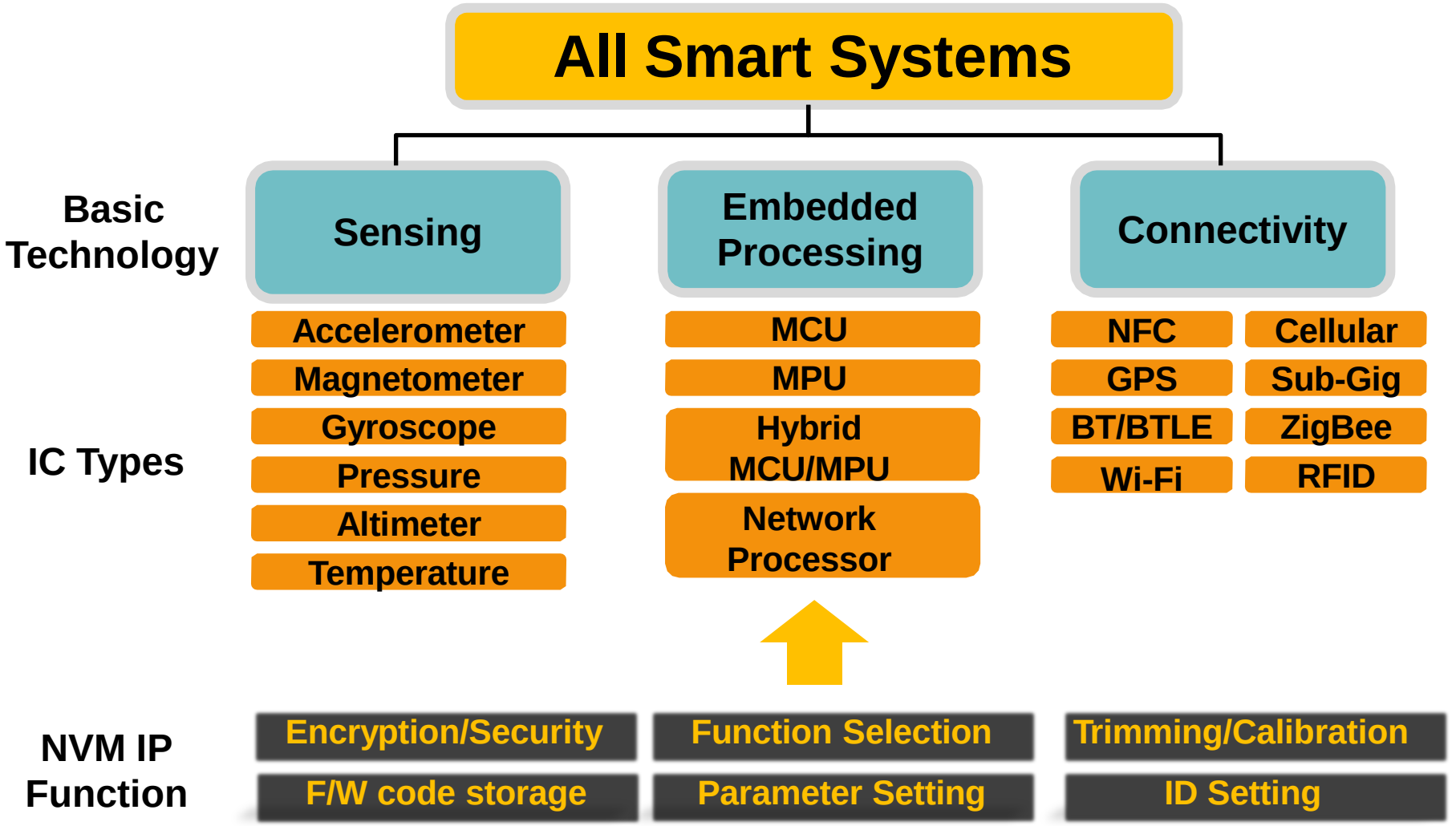
OTP for security storage



Source： Rambus crypto manager platform

Security with eMemory IPs

NVM IP Demand in IoT

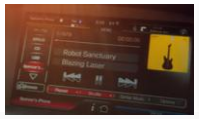


Autotronics with eMemory IPs

Intelligent drive
Distronic system

Neo **Bit** Neo **Fuse**

Infotainment system

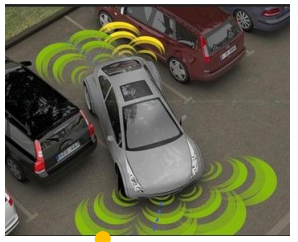


Neo **Bit** Neo **Fuse**

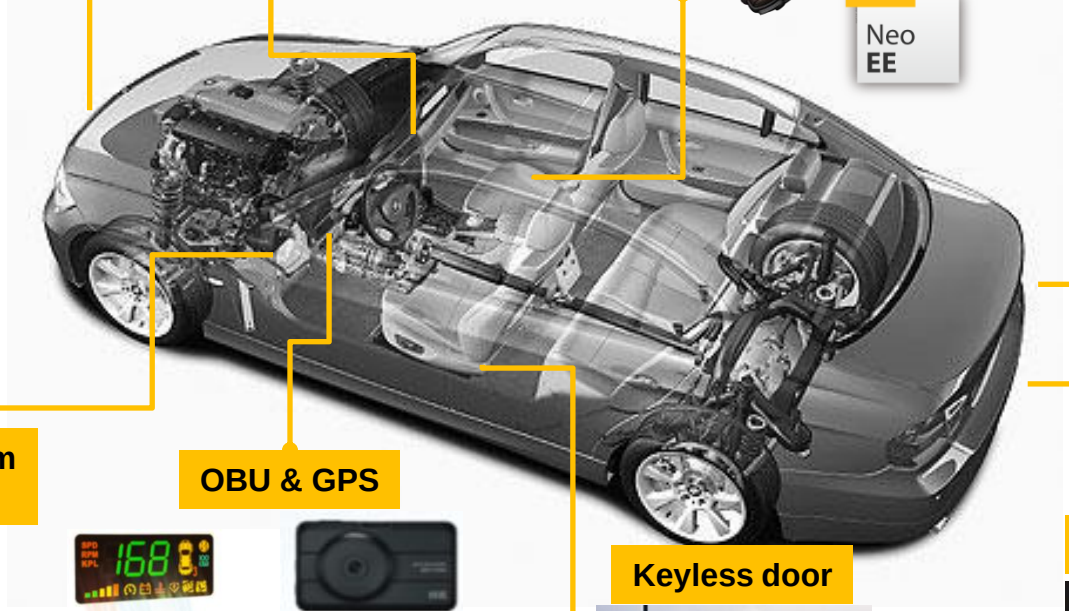
Sensor system

Neo **Bit** Neo **EE**

Auto parking system



Neo **Bit** Neo **Fuse**



Blind Spot Warning System
Cockpit System

Neo **Bit** Neo **Fuse**

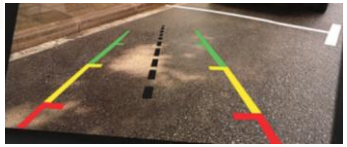
OBU & GPS

Neo **Bit** Neo **Fuse**

Keyless door

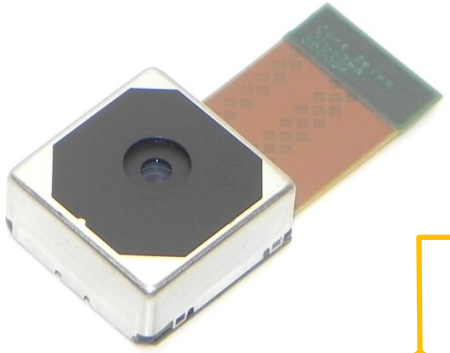
Neo **Bit** Neo **EE**

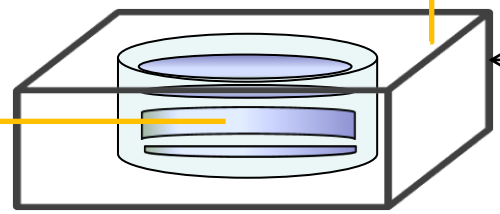
Rear view system

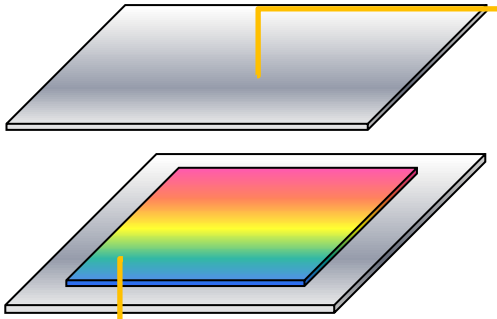


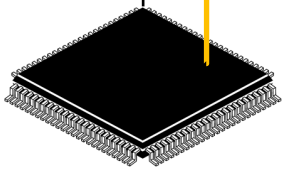
Neo **Bit** Neo **Fuse**

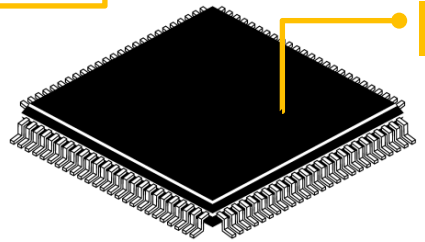
Imager Module with eMemory IPs











VCM

Lens

IR Cut Filter

AF/OIS Controller
(VCM Driver)

Neo Fuse

Neo Bit

Neo EE

Neo MTP

Image Sensor

Neo Fuse

Neo Bit

ISP

Neo Fuse

Neo Bit

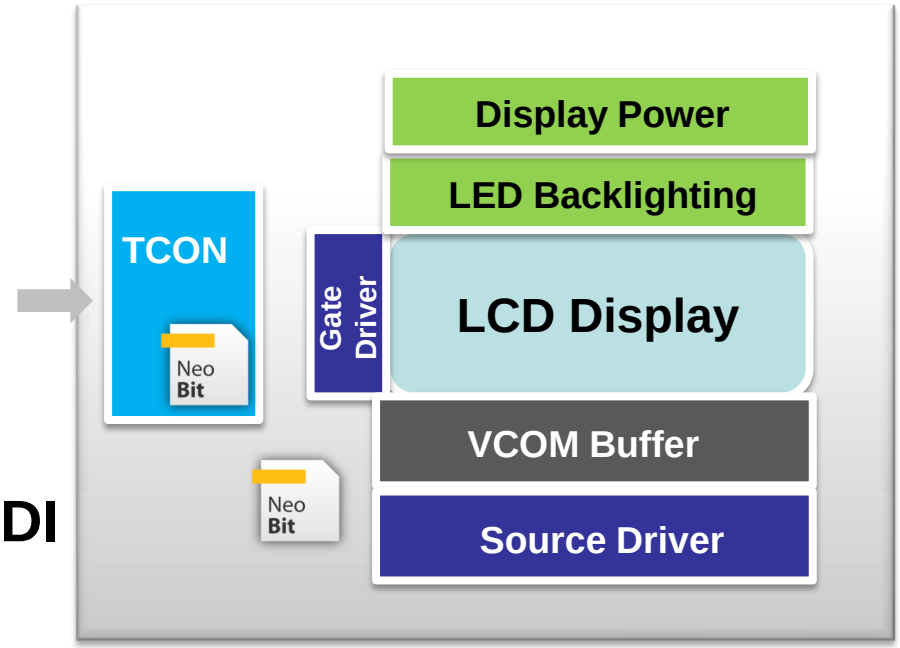
Neo EE

Neo MTP

Advanced LCD Driver ICs

Process Technology : 0.11um HV/80nm HV/55nm HV

I/F
(LVDS, MIPI,…)

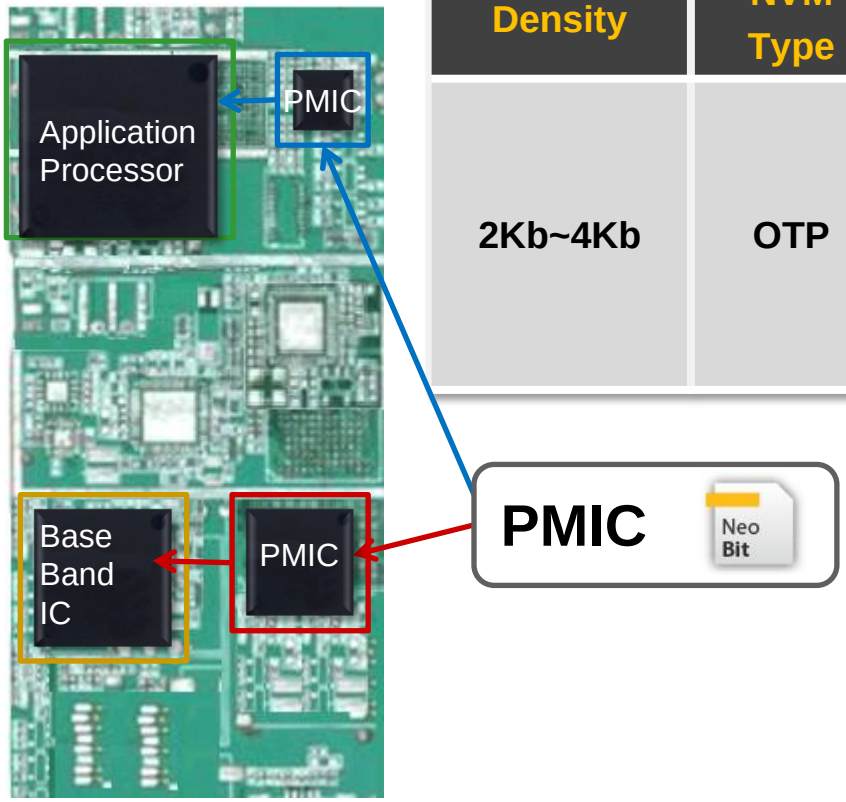


DDI

Density	Endurance	NVM Type	Purpose	NVM Usage
2K8~4K8	1	OTP	Trimming	1. Accuracy enhancement 2. Mismatch cancellation
			Code Storage	1. Gamma Correction Table 2. Timing Control Pattern 3. Color Engine Enhancement

Power Management ICs for Baseband and Application Processor

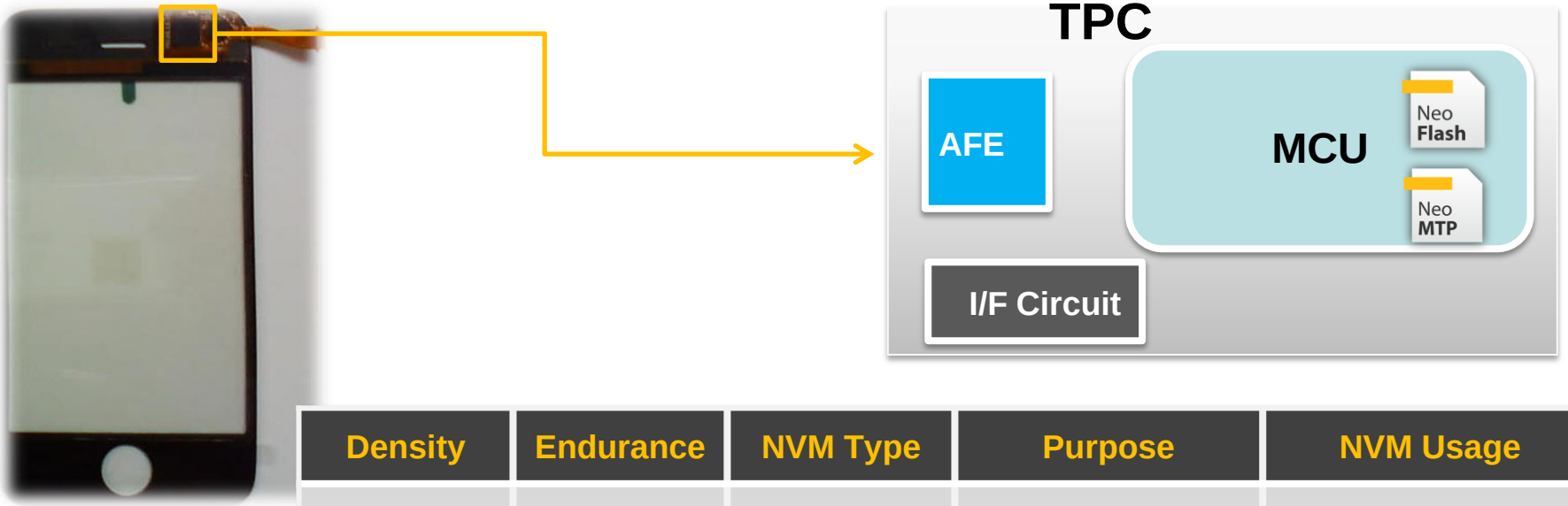
Process Technology : Advanced 0.25um BCD/ 0.18um BCD/ 0.13um BCD
Mature 0.18um/0.16um/0.152um Logic



Density	NVM Type	Purpose	NVM Usage
2Kb~4Kb	OTP	Trimming	DC/DC, Bandgap
		Parameter Setting	Design flexibility & Performance optimization
		Code Storage	Start-up behavior & smart power saving algorithm

Touch Panel Controller ICs

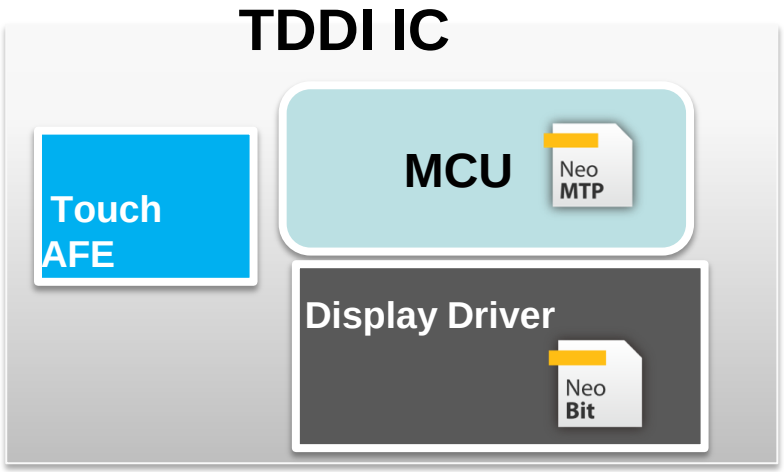
Process Technology : 0.16um HV/0.11um G



Density	Endurance	NVM Type	Purpose	NVM Usage
16K8~32K8	<1000	MTP	Code Storage	F/W code
			Parameter setting	Customized model and performance optimization

In-Cell Touch Panel Controllers ICs

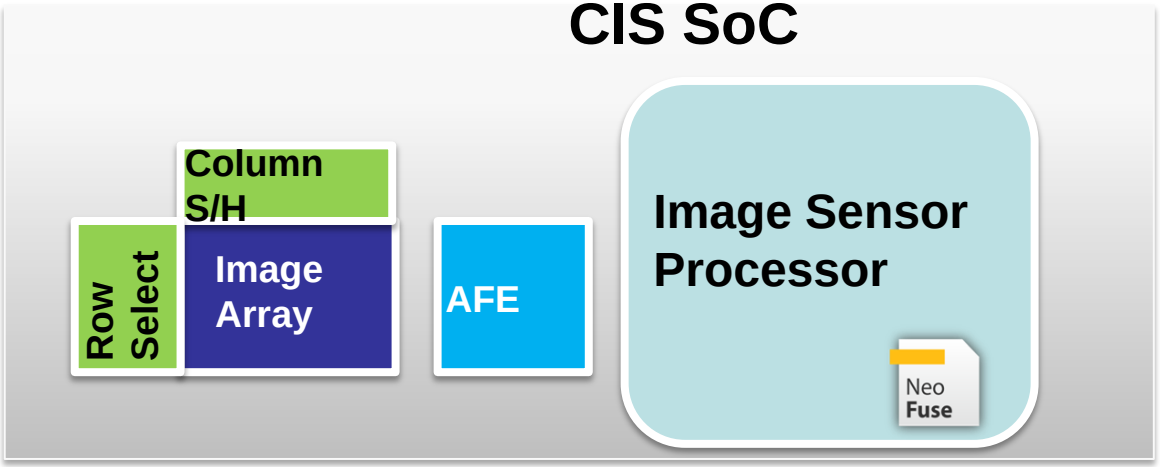
Process Technology : 0.11um HV/80nm HV/55nm HV

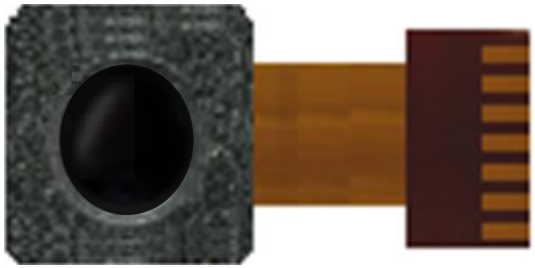


Density	Endurance	NVM Type	Purpose	NVM Usage
2K8~4K8	1	OTP	Trimming	Accuracy
			Code Storage	Gamma Table
16K8~32K8	<1000	MTP	Code Storage	Touch F/W Code
			Parameter setting	Performance Optimization

CMOS Image Sensor

Process Technology : 0.11um CIS/90nm CIS/65nm CIS

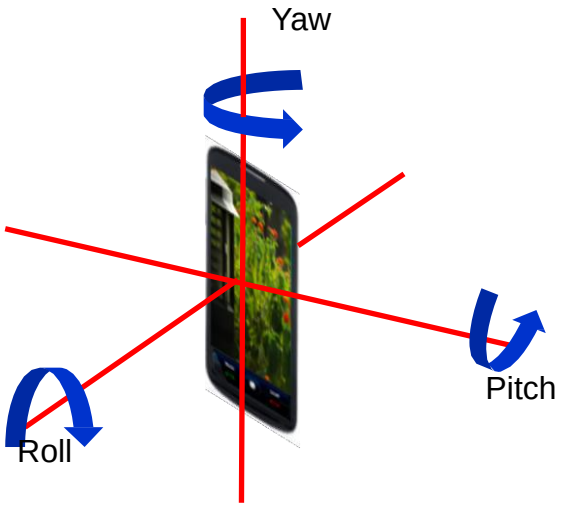


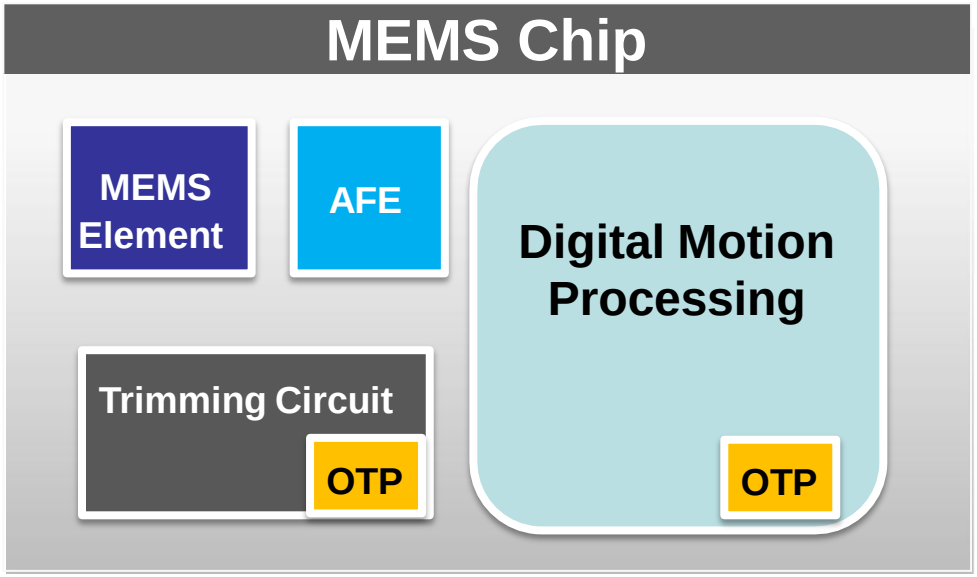


Density	Endurance	NVM Type	Purpose	NVM Usage
2Kb~4Kb	1	OTP	Identification Setting	Product Code
			Parameter Setting	Start-up Initial Setting
32K8	1	OTP/ROM	Code Storage	Boot Load

MEMS

180/160/15x nm HV/Logic for MEMS Controller





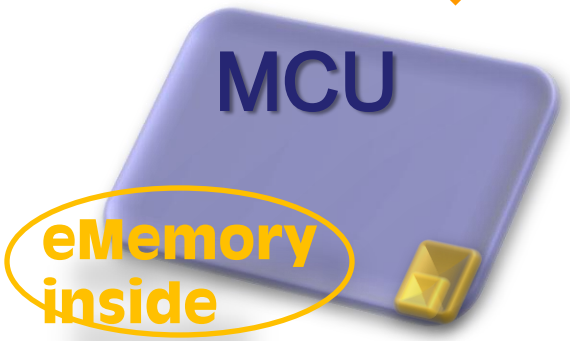
Density	NVM Type	Purpose	NVM Usage
2Kb~4Kb	OTP	Trimming	Factory trimming
		Parameter Setting	Signal filtering
		Code Storage	Geometric computation

Replacement of Embedded Flash for Competitiveness Improvement

product design & manufacturing by embedded Flash
Logic Process + 10 Masks

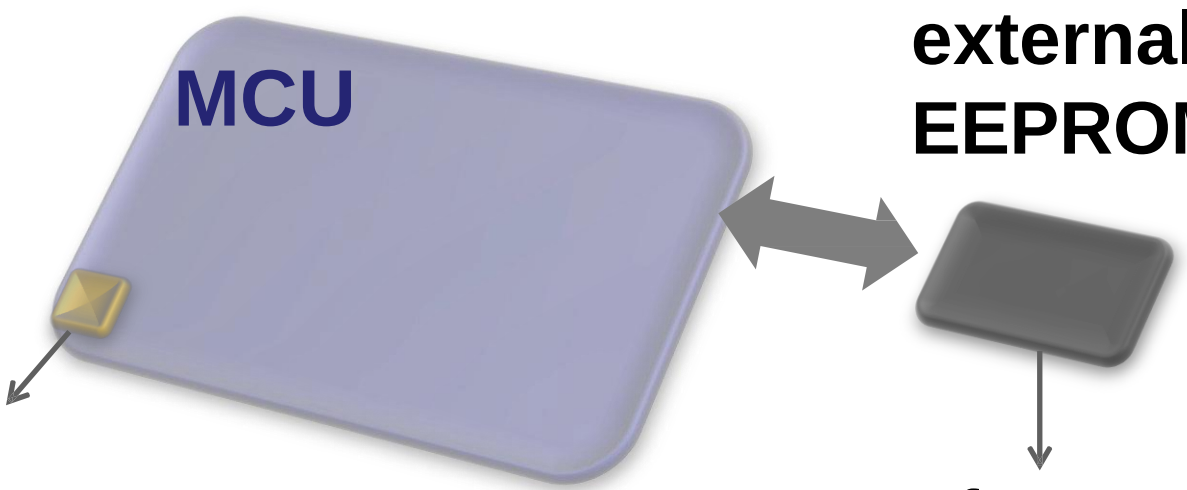
30% more cost reduction

wafer cost & testing time



product design & manufacturing by Embedded Logic NVM (OTP/MTP) Logic Process

MCU Applications with EEPROM

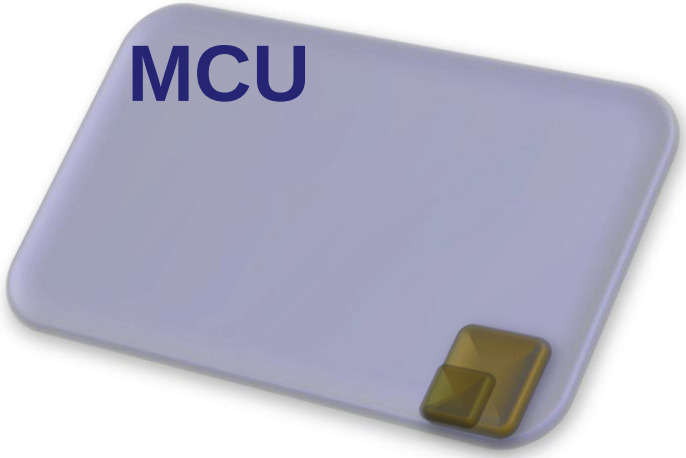


One-time storage for ID, trimming, encryption…

EEPROM for user data, parameter setting, system function…

NeoBit + NeoEE

Hybrid NVM solution (NeoBit + NeoEE) with customized SPEC & optimized size



- **One single IP by integration of NeoBit & NeoEE**
- **Help for system size reduction**

Wafer Demand by IC Type

IC Type	Equa to 8-inch wafer (K)
AP	5740
PMU	5255
Base Band controller	2945
Smart card controller	2683
Fingerprint	2500
CIS sensor	2215
LCD driver (int with TCON)	1955
Gauge IC	708
TV controller	619
Touch panel controller (C)	602
Connectivity	463
STB controller	348
DC-DC/AC-DC	239
Wifi controller	231
Accelator sensor controller	166
LED driver	140
Light snesor	126
Gyroscope sensor controller	120
BT controller	107
TAG IC	104
MCU (8bits, LV/3.3V)	90
MCU (8bits, pure 5V)	88
ISP	82
DVD controller	67
P-Gamma	47
NB CAM controller	38
Pressure sensor controller	23
Touch pad controller	16
PC CAM controller	14
Touch panel controller (R)	3
TCON (w/o driver)	3
Speech controller	0

2015 Q3 updated

Outlook for Q4 and Beyond

- License fee expected to grow due to the successful development in advanced nodes.
- PMIC continually extends to the application of wireless charger and fast charger related products.
- 55nm DDI continues volume production. More than 50 tape out were done in past two years.
- 28nm Set-top Box processor starts to volume production. There are more customers will tape out new products in Q1 2016.

Outlook for Q4 and Beyond

- Fingerprint and CIS customers start to small volume production.
- The qualification of 16nm FF^{+} started and expected to be completed at end of March 2016.
- 16nm FFC verification is successful. Qualification will be started in Q1 2016.
- 10nm FF IP will tape out in March and already has customer engagement.
- More projects on automotive, the applications extend from PMIC to LCD Driver.

Key Growth Drivers

Growth in application per mobile devices	• More chip applications per smartphone/tablet product.
Growth into more markets	• From consumer electronics and mobile devices to wearable devices. • Adding new NVM product lines further enable more product applications.
Growth in advanced technology	• Higher royalty per wafer is contributed from more advanced technology nodes.
Great IoT era	• Embedded Logic NVM will be a must.

Q & A

ememory

Embedded Wisely, Embedded Widely