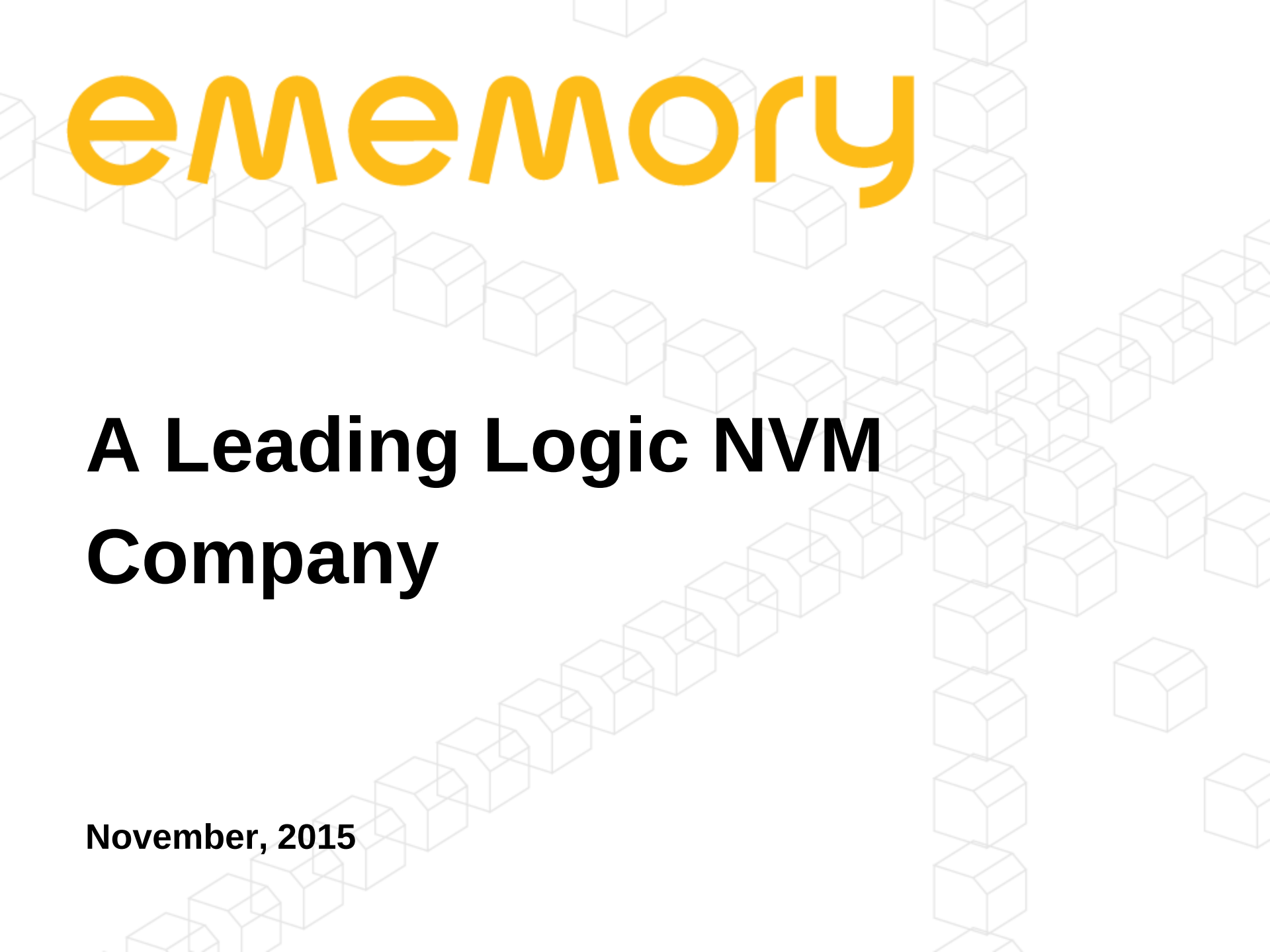


The background of the slide is filled with a pattern of white, 3D-outlined cubes. These cubes are arranged in a way that creates a sense of depth and movement, with some cubes appearing to be in the foreground and others receding into the background. The cubes are scattered across the entire slide, creating a textured, geometric backdrop.

ememory

A Leading Logic NVM Company

November, 2015

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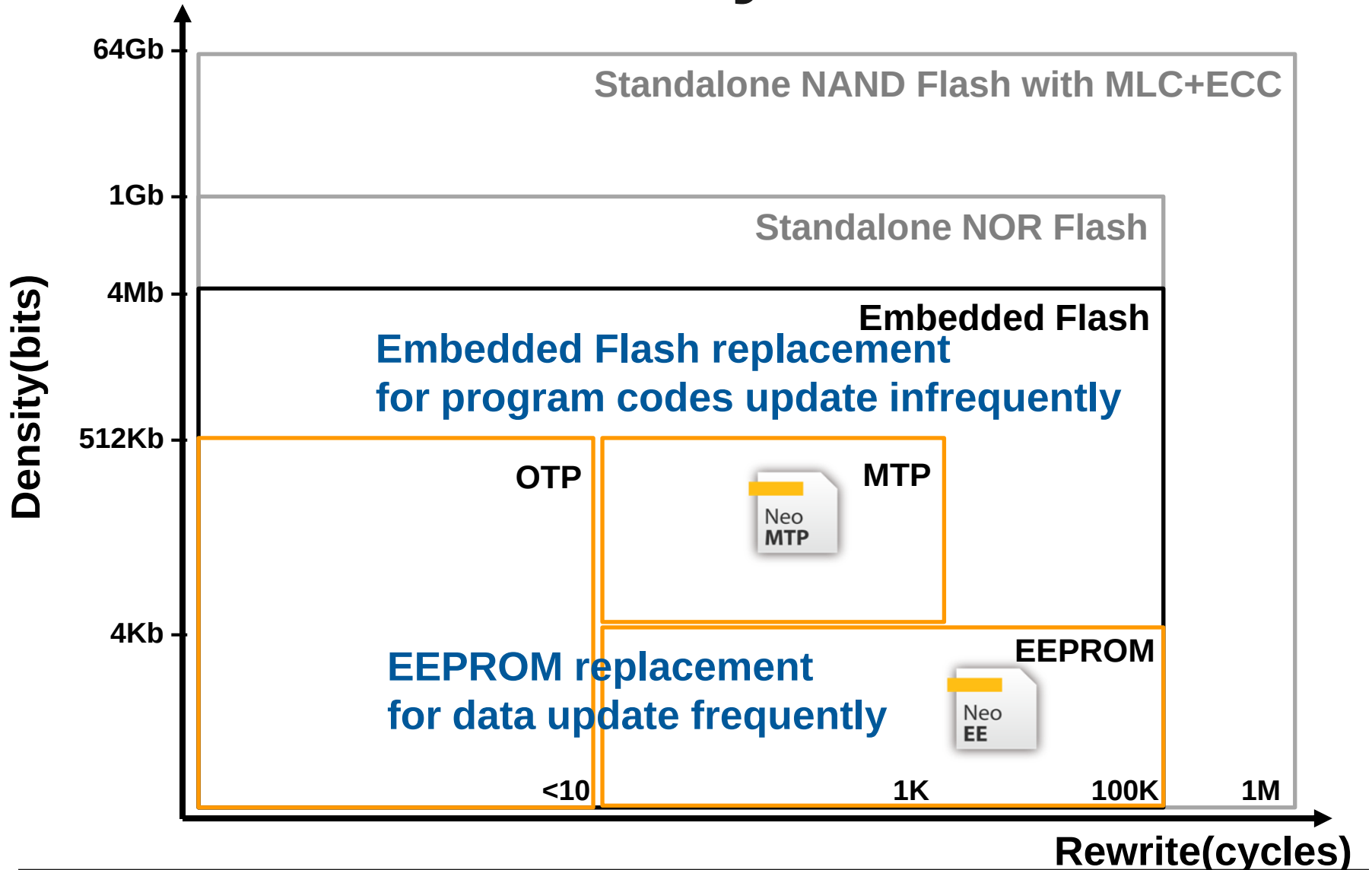
Cautionary Statement

This presentation contains forward-looking statements, which are subject to risk factors associated with semiconductor and intellectual property business. It is believed that the expectations reflected in these statements are reasonable. But they may be affected by a variety of variables, many of which are beyond our control. These variables could cause actual results or trends to differ materially and include, but are not limited to : wafer price fluctuation, actual demand, rapid technology change, delays or failures of customers' tape outs into wafer production, our ability to negotiate, monitor and enforce agreements for the determination and payment of royalties, any bug or fault in our technology which leads to significant damage to our technology and reputation, actual or potential litigation, semiconductor industry cycle and general economic conditions. Except as required by law, eMemory undertakes no obligation to update or revise any forward-looking statements, whether as a result of new information, future events, or otherwise.

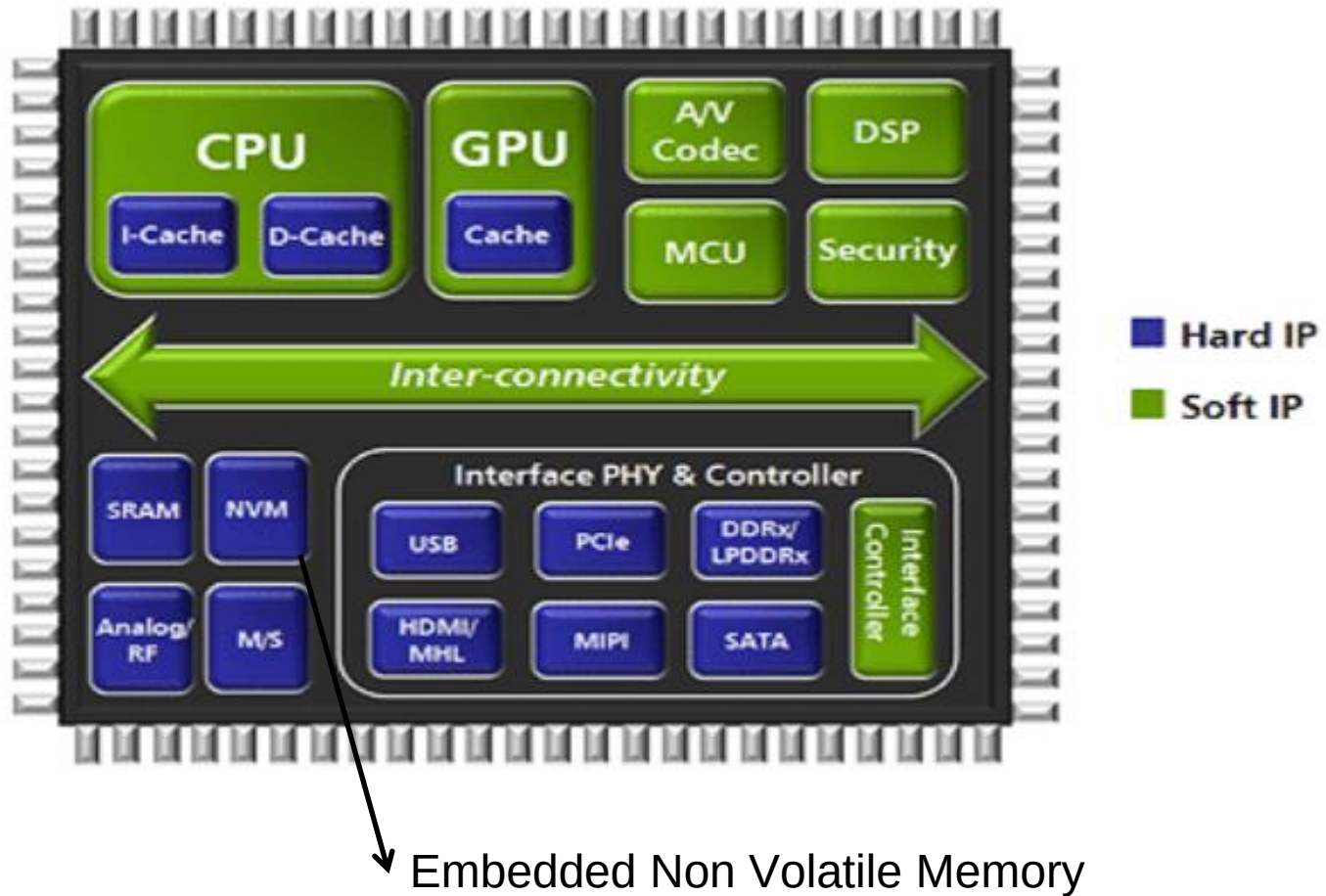
Outline

- **Business Model**
- **Review of Operations**
- **Growth Opportunity and Future Outlook**
- **Q & A**

Nonvolatile Memory Classifications



SOC Block Diagram



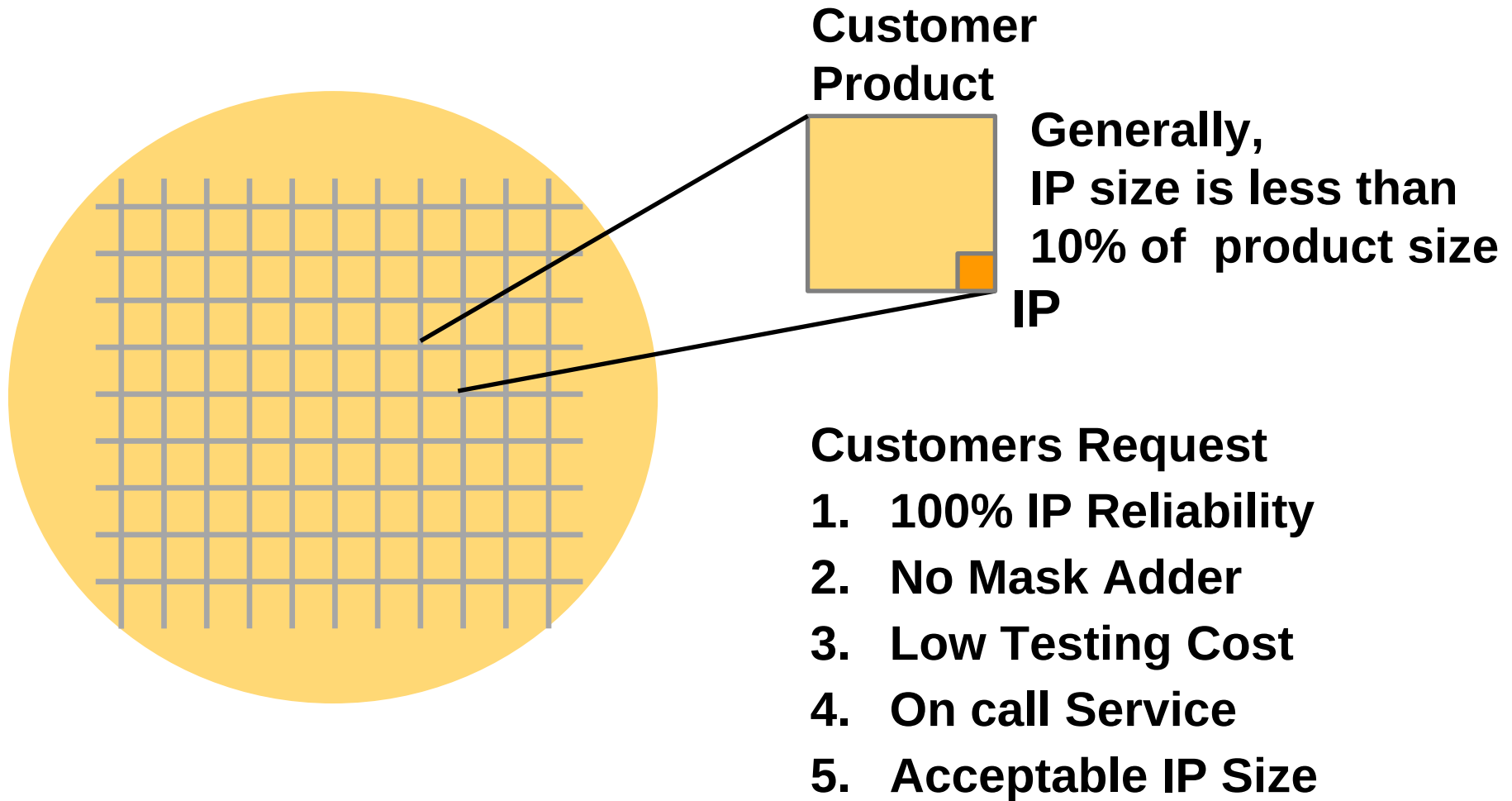
Source : tsmc

Embedded NVM Technologies

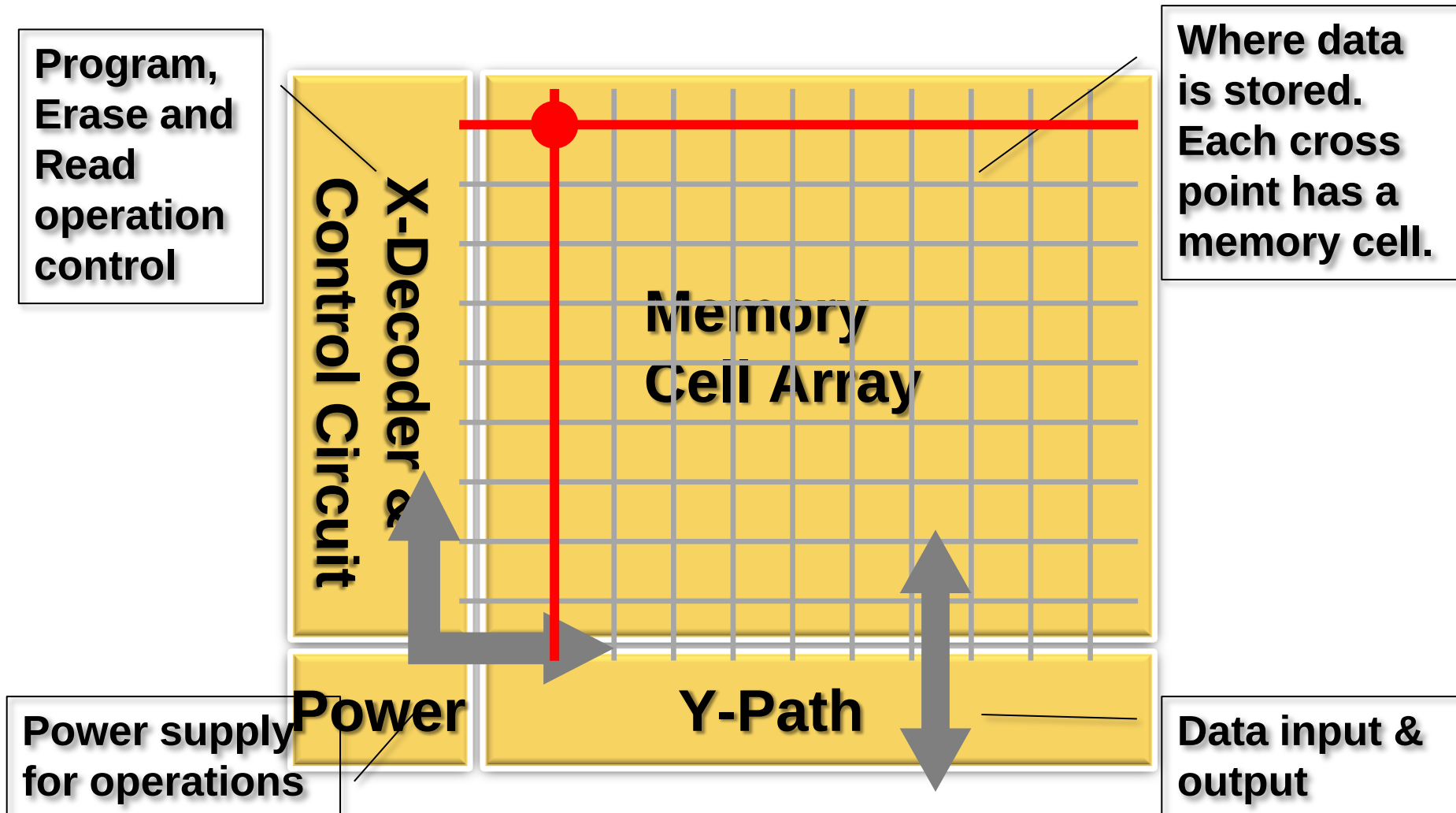
	ROM	eFuse (OTP)	Antifuse (OTP)	CMOS Floating Gate (OTP)	CMOS Floating Gate (MTP)	Embedded Flash
Cell Structure	Transistor	Poly Fuse	Antifuse	Floating Gate	Floating Gate	Floating Gate
Standard CMOS Compatible	Yes	Yes	Yes	Yes	Yes	No
Bitcell Area	< 1	50	1	2	4	1
Endurance	No	No	< 10	< 10	10K-100K	100-1000K
Density	4Kb-1Mb	256bit-4Kb	16bit-1Mb	16Kb-1Mb	1Kb-2M	64Kb-4Mb
Security	Low	Low	High	High	High	High
Additional Steps	None	None	None	None	None	+10 Mask

- ROM not programmable, eFuse cannot scale beyond 16Kb, embedded flash expensive and cannot scale after 40 nm
- eMemory's IPs: OTP (antifuse, floating gate) and MTP (floating gate)

Considerations for IP Adoption

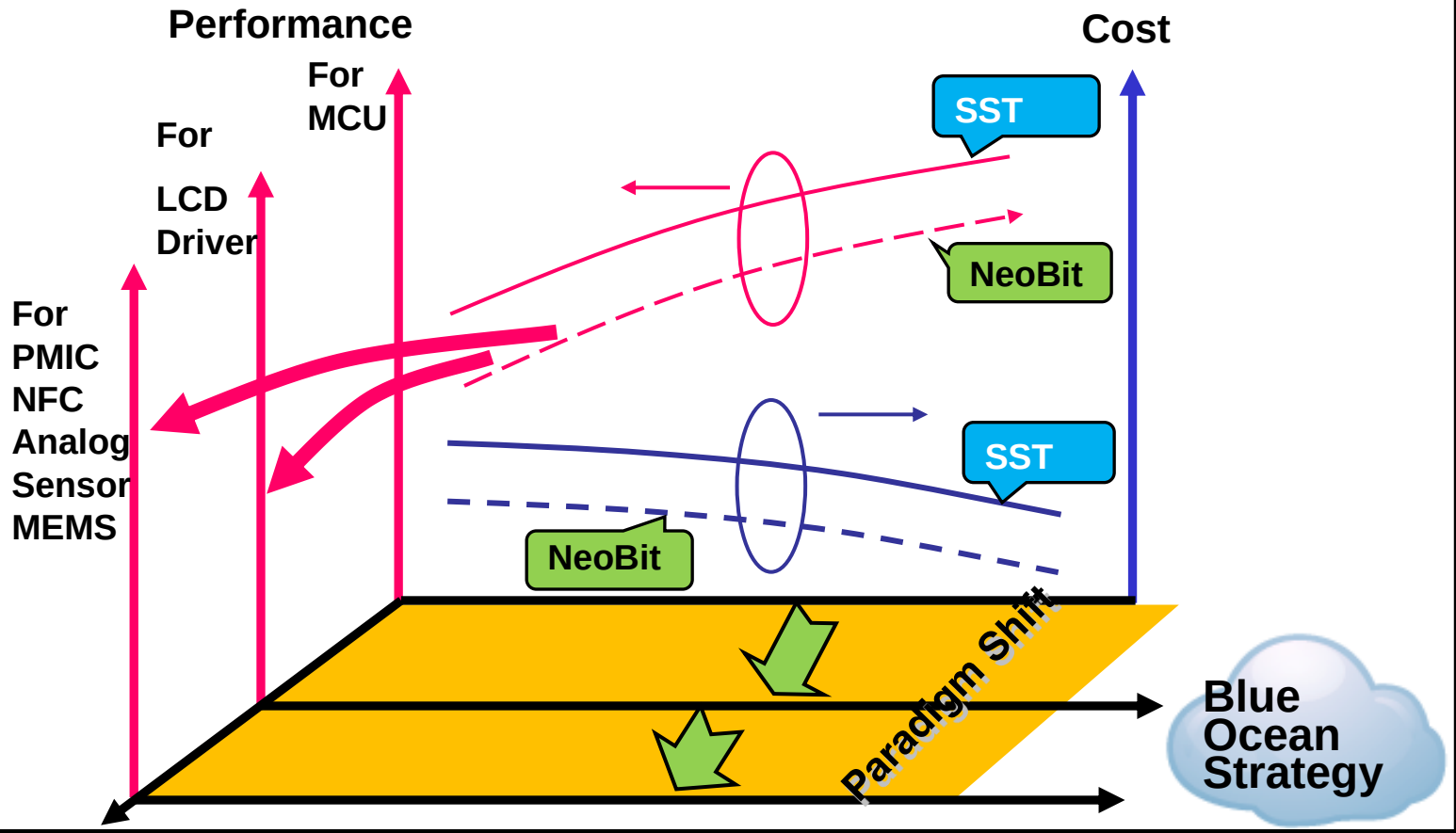


Inside Nonvolatile Memory IP

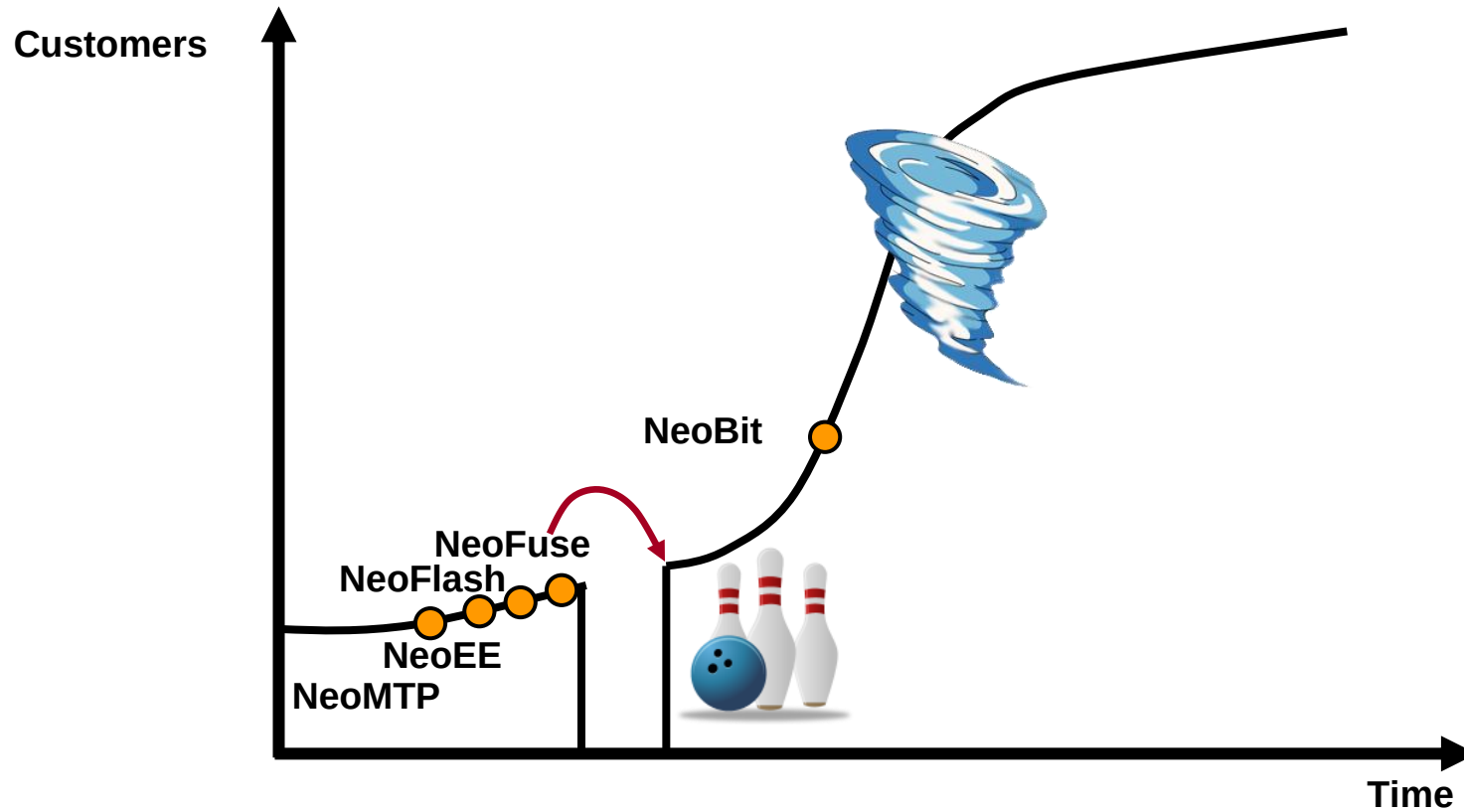


What We Have Done

● *Innovation, Innovation, and Innovation !*



Crossing the Chasm



Business Model

- Founded in 2000. First customer engaged in 2002. Achieved profitability in 2005 and IPO in 2011. The largest logic non-volatile memory IP company, 224 employees (155 R&D)*.
- Since its IPO, the company initiated no new fund raising or bank debt, and has distributed in excess of 100% of earnings in cash dividends.
- **Growth Indices:** 1) No. of on-going technology platforms
2) No. of design licenses
3) Royalty



Note*: As of Oct. 31, 2015

Worldwide Customers



Foundry



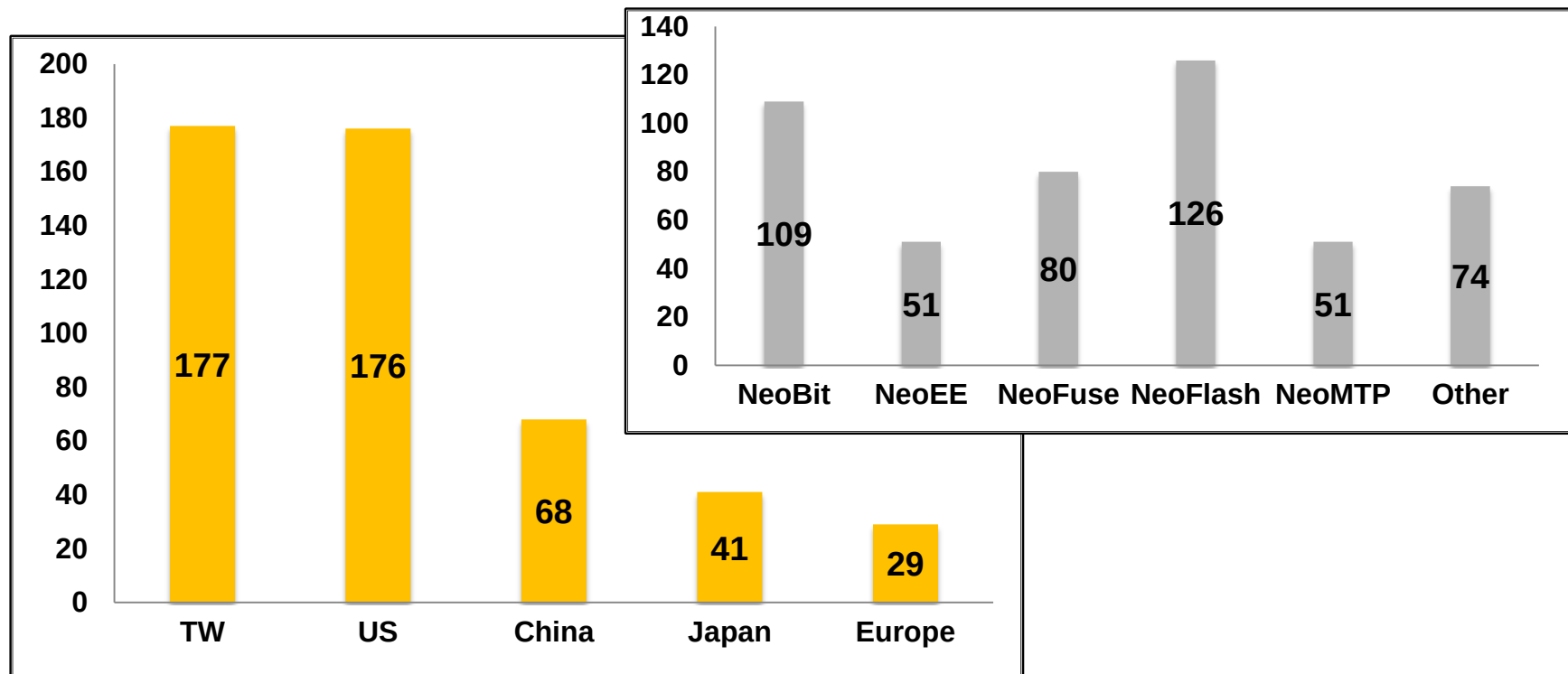
IDM



	Taiwan	China	Korea	Japan	North America	Europe	Others
Foundry	5	7	3	2	1	1	1
IDM	0	0	0	8	2	1	0
Fabless	237	351	51	36	181	94	40

Patent Portfolio

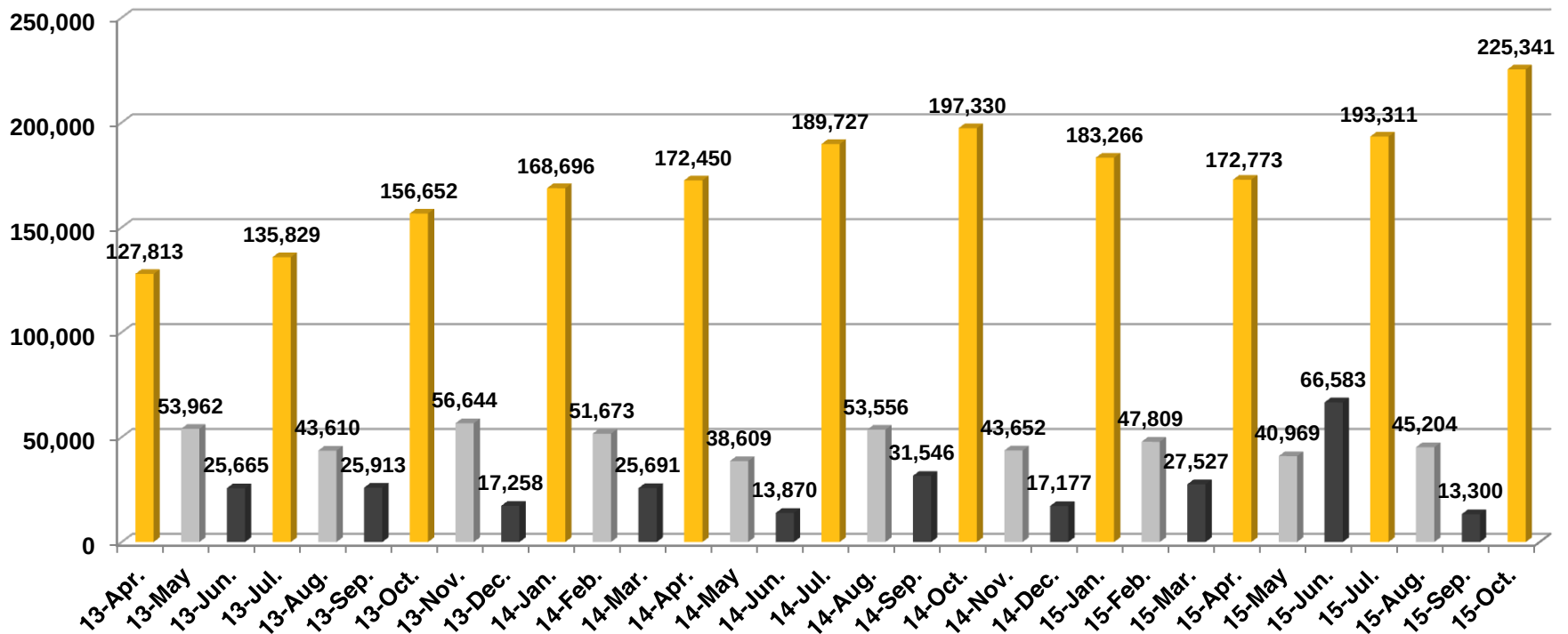
	Q215	Q315	Diff.
Pending	181	187	+6
Issued	287	304	+17
Total	468	491	+23



Quarterly Revenue Pattern

- The quarterly royalty from most of foundries are collected at first month of each quarter and from some other foundries are collected at second month, and none at third month.

Unit : NTD Thousands



Outline

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Q3 Revenue Breakdown

Unit: NTD thousands

	Q315	Q215	% change	Q314	% change	2015Q1-Q3	2014Q1-Q3	% change
Licensing	38,167	95,982	-60.24%	61,981	-38.42%	198,205	194,224	2.05%
Royalty	213,648	184,343	15.90%	212,848	0.38%	592,537	551,594	7.42%
Total	251,815	280,325	-10.17%	274,829	-8.37%	790,742	745,818	6.02%

Unit: Number of contracts

	Q315	Q215	2014	2013
Technology Licenses	4	8	21	19
Design Licenses				
NRE	10	17	82	51
Usage	76	87	363	342

Financial Income Statement

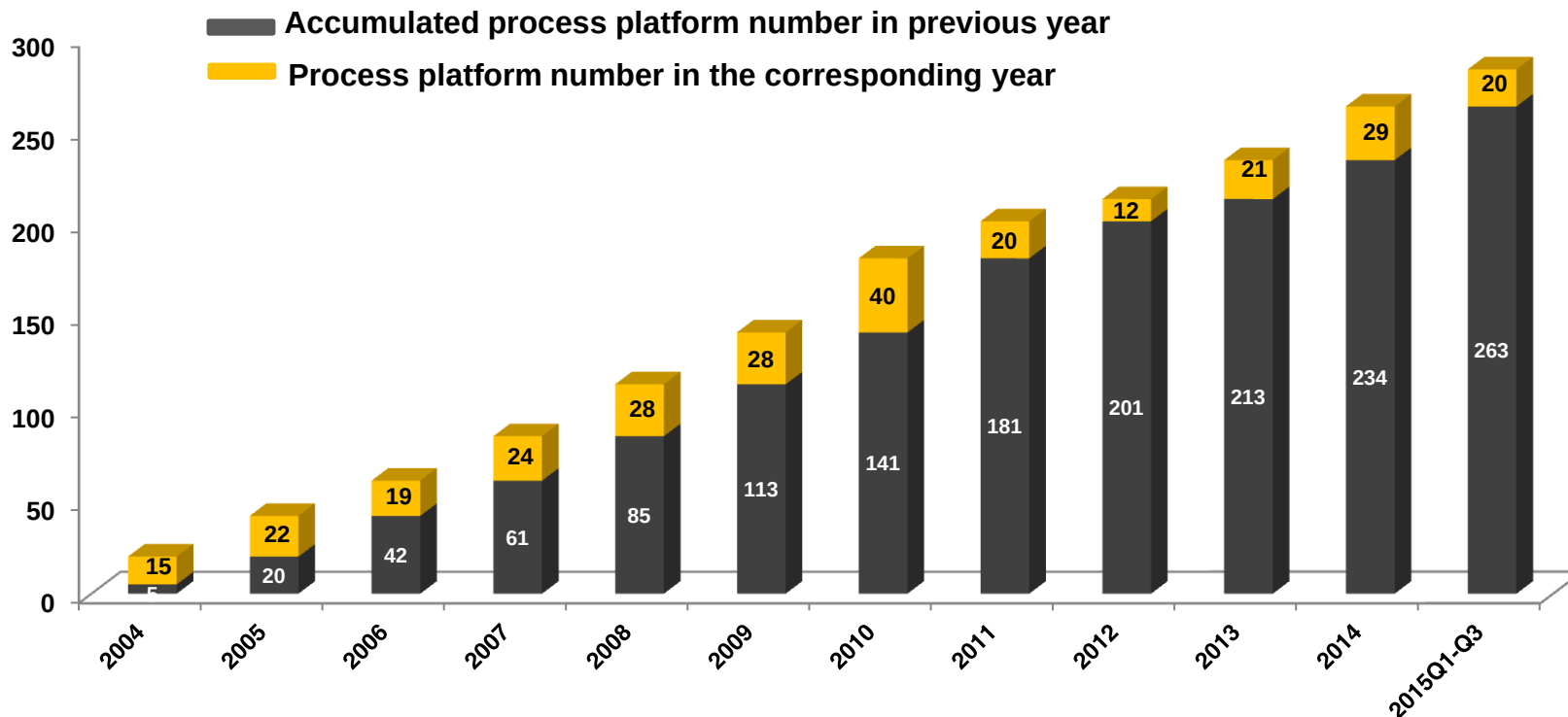
(Unit: NTD thousands)	Q315	Q215	% change	Q314	% change
Revenue	251,815	280,325	-10.17%	274,829	-8.37%
Gross Margin	100%	100%	-	100%	-
Operating Expenses	143,776	141,435	1.66%	135,695	5.96%
Operating Margin	42.9%	49.5%	-6.6ppts	50.6%	-7.7ppts
Net Income	106,301	130,297	-18.42%	124,352	-14.52%
Net Margin	42.2%	46.5%	-4.3ppts	45.2%	-3.0ppts
EPS (Unit: NTD)	1.40	1.72	-18.60%	1.64	-14.63%
ROE	24.5%	30.9%	-6.4ppts	29.7%	-5.2ppts

Technology License

Unit: Number of contract

Year	2013	2014	2015Q1-Q3
License number	19	21	17

Note: The terms (including number of process platforms and licensing fees) for each technology license are set contractually. Payments are made according to set milestones, and there are no particular seasonal factors involved.



Current Technology Development Platforms

- Total (As of Sep.) : **83***
- **17** for NeoBit, **28** for NeoFuse, **23** for NeoEE, and **15** for NeoMTP.

	14/16nm	28nm	40nm	55/65nm	80/90nm	0.11~ 0.13um	0.15~ 0.18um	>0.25 um	Total
NeoBit	-	-	-	-	-	5	11	1	17
NeoFuse	2	6	4	8	2	4	2	-	28
NeoFlash	-	-	-	-	-	-	-	-	-
NeoEE	-	-	2	-	1	6	14	-	23
NeoMTP	-	-	1	1	2	3	8	-	15

Note*: 5 platforms qualified in Q3, 4 platforms kicked off in Q3

Current Technology Development Platforms

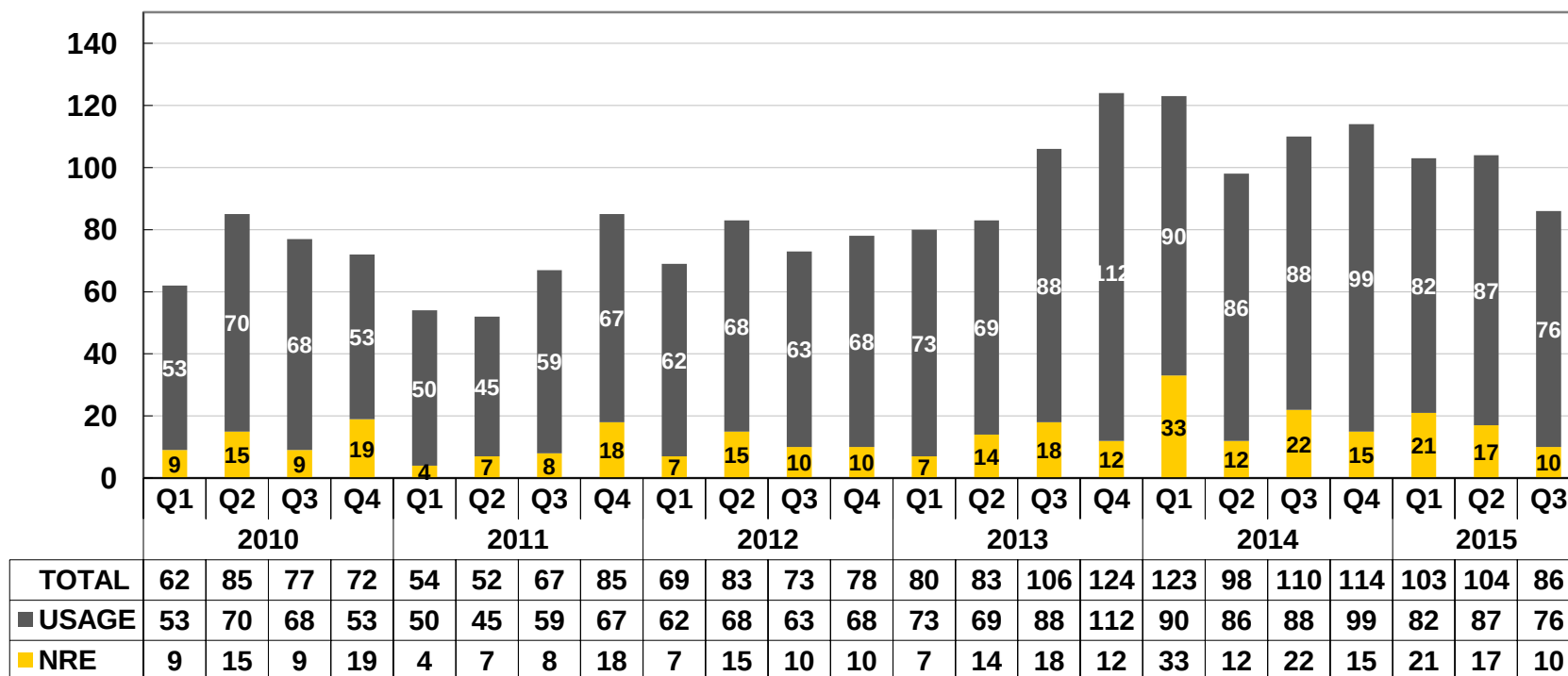
12" Fabs	Production	Development	NVM Type	Process Type
16nm	0	2	OTP	FF+
28nm	4	6	OTP	LP/HPM, HLP/HPM, LPS
40nm	2	7	OTP, MTP	HV-DDI, LP
55/65nm	10	9	OTP, MTP, Flash	LP, HV-DDI, HV-OLED, DRAM, CIS
80/90nm	5	5	OTP, MTP	HV-DDI, HV-OLED, LP
0.13/0.11um	6	4	OTP, Flash	HV-DDI, BCD, Generic
0.18um	1	0	OTP	BCD

8" Fabs	Development	NVM Type	Process Type
0.13/0.11um	14	OTP, MTP, Flash	HV-DDI, BCD, LP, RF, CIS, LL
0.18/0.16/0.152um	35	OTP, MTP	Generic, LP, LL, MR, HV, Green, BCD
0.25um	1	OTP, MTP	BCD
0.35um	0	OTP	UHV

*As of Sep. 30, 2015

Quarterly Design Licensing (New Tape Out)

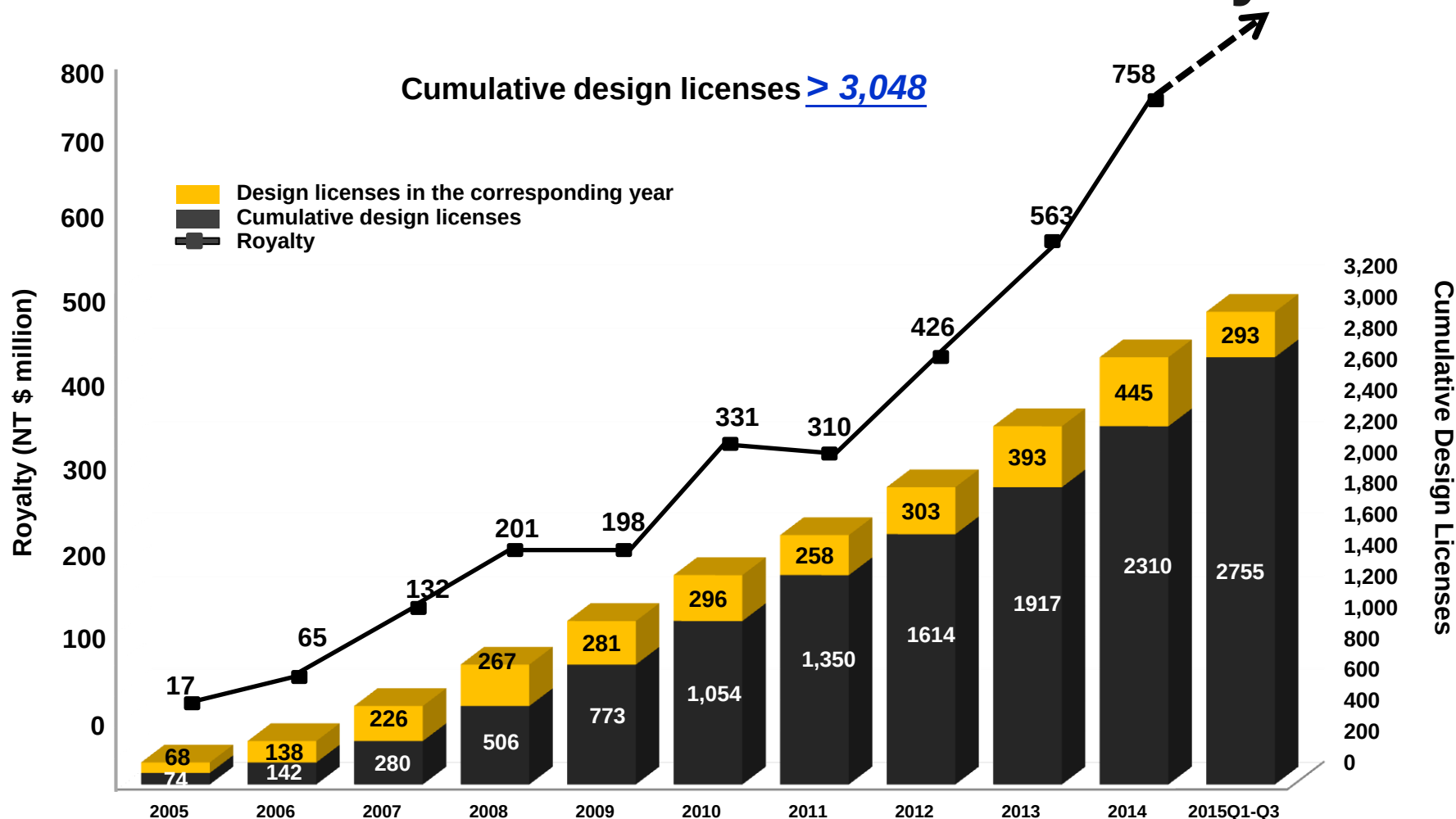
- Total **293** NTO as of Q3 2015 (**445**@2014 **393**@2013, **303**@2012, **258**@2011)



Usage : Usage of pre-qualified and verified IP (charged by per product tape out or annual package), the cycle time from design implementation to royalty payments for mass production is faster, typically less than one year.

NRE: NRE covers the customization of IP that must undergo new verification or qualification. It typically requires 1 to 1.5 years before resulting in royalty revenue.

Cumulative Licenses Drive Future Royalties

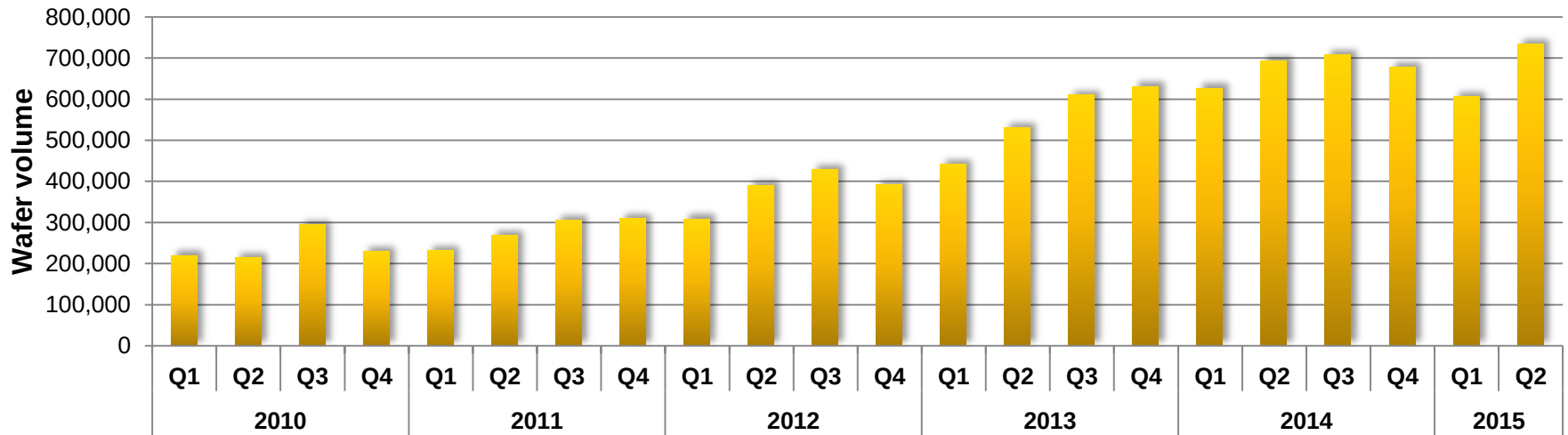


note 1: Due to the 2009 recession, royalty income was down annually 1.5%.

note 2: Pre-payment of royalty fees by a single customer contributed to 2010 annual growth of 67%, causing a drop of 6.3% in the following year, 2011.

note 3: CAGR for 2009-2013 was 30%.

Wafer Production Volume



embedded eMemory IP in T Company (\$revenue); * % of Process node in T company total revenue in Q315

	Process node	*% of T	Q315	Q215	2014	2013
8"	0.25/0.35	4%	38.2%	34.4%	30.5%	27.3%
	0.15/0.18	12%	7.9%	8.9%	11.9%	10.7%
	0.11/0.13	2%	30.9%	17.0%	20.8%	19.1%
12"	90nm	8%	21.8%	19.2%	16.3%	4.8%
	65nm	11%	0.9%	0.4%	0%	0%
	40/45nm	14%	0%	0%	0%	0%
	28nm	27%	0.02%	0.01%	0%	0%
	16/20nm	21%	0%	0%	0%	0%
8"		19%	16.3%	14.5%	15.6%	14.2%
12"		81%	2.3%	1.8%	1.4%	0.69%
Total		100%	5.0%	4.5%	4.5%	4.1%

Outline

- **Business Model**
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- **Q & A**

eMemory's NVM Technologies

- **Logic NVM portfolio offers one-stop-shop solution.**
 - › Compatible to any process
 - › Robust structure
 - › Low process cost
 - › Competitive macro sizes
 - › Easy integration
 - › Easy porting

eMemory's NVM Technology	OTP			MTP	
	NeoBit	NeoFuse	NeoFlash	NeoEE	NeoMTP
Product Type	OTP	OTP	Flash	EEPROM	MTP
Endurance (Cycles)	10	10	1K~10K	10K~100K	1K~10K
Additional Mask Steps	0	0	2-3	0	0
Technology	Floating gate	Anti-Fuse	SONOS	Floating gate	Floating gate
Scalability	Simple	Simple	Simple	Simple	Simple
Memory Density	HD < 512Kb GHD < 16Mb	< 4Mb	< 2Mb	< 4Kb	< 512Kb

Applications by Technology

12"

8"

16/20nm

28nm

40nm

55/65nm

80/90nm

110/130nm

160/180nm

250nm

350nm

NeoBit

NeoFuse

NeoFlash

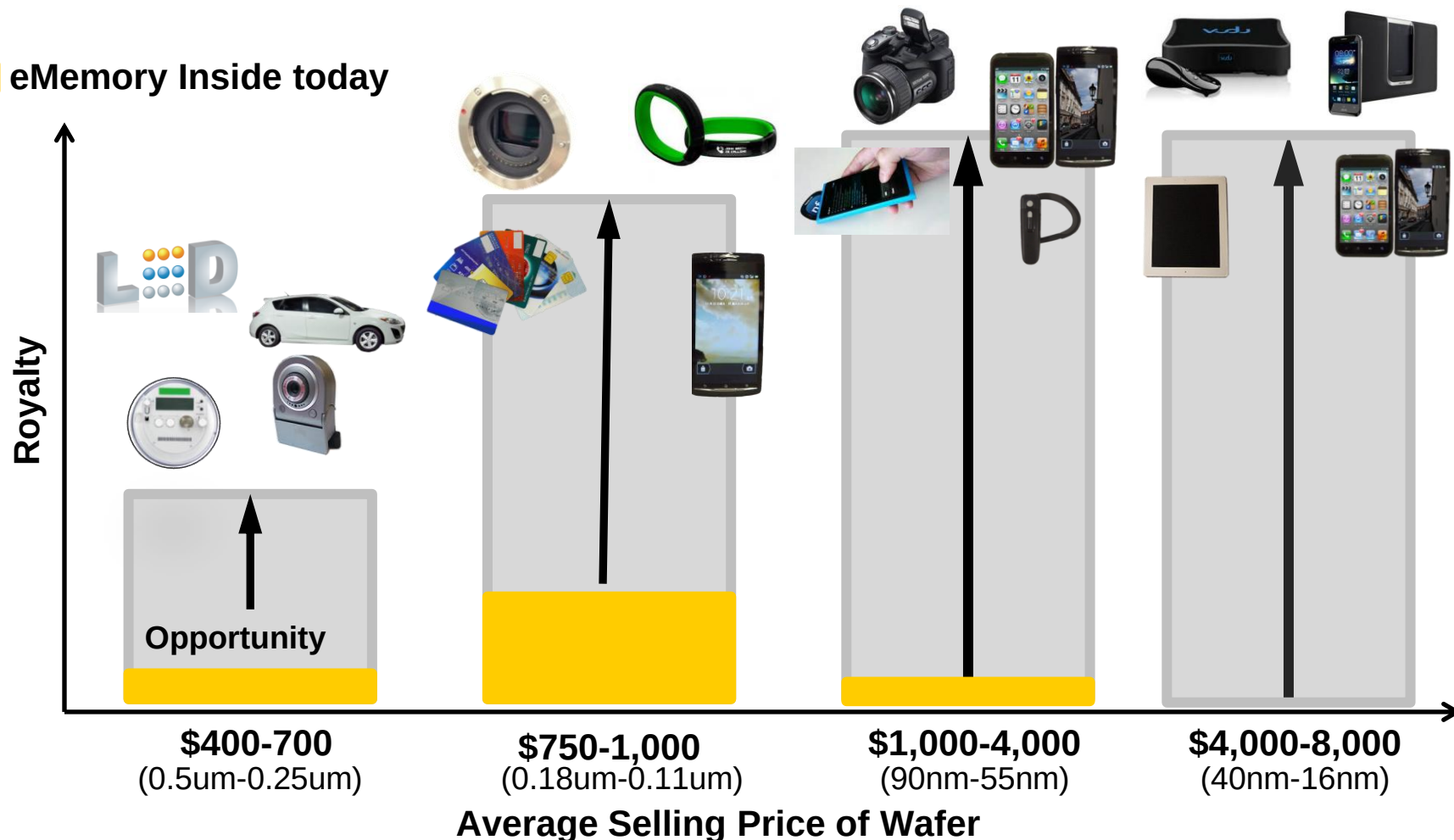
NeoEE

NeoMTP



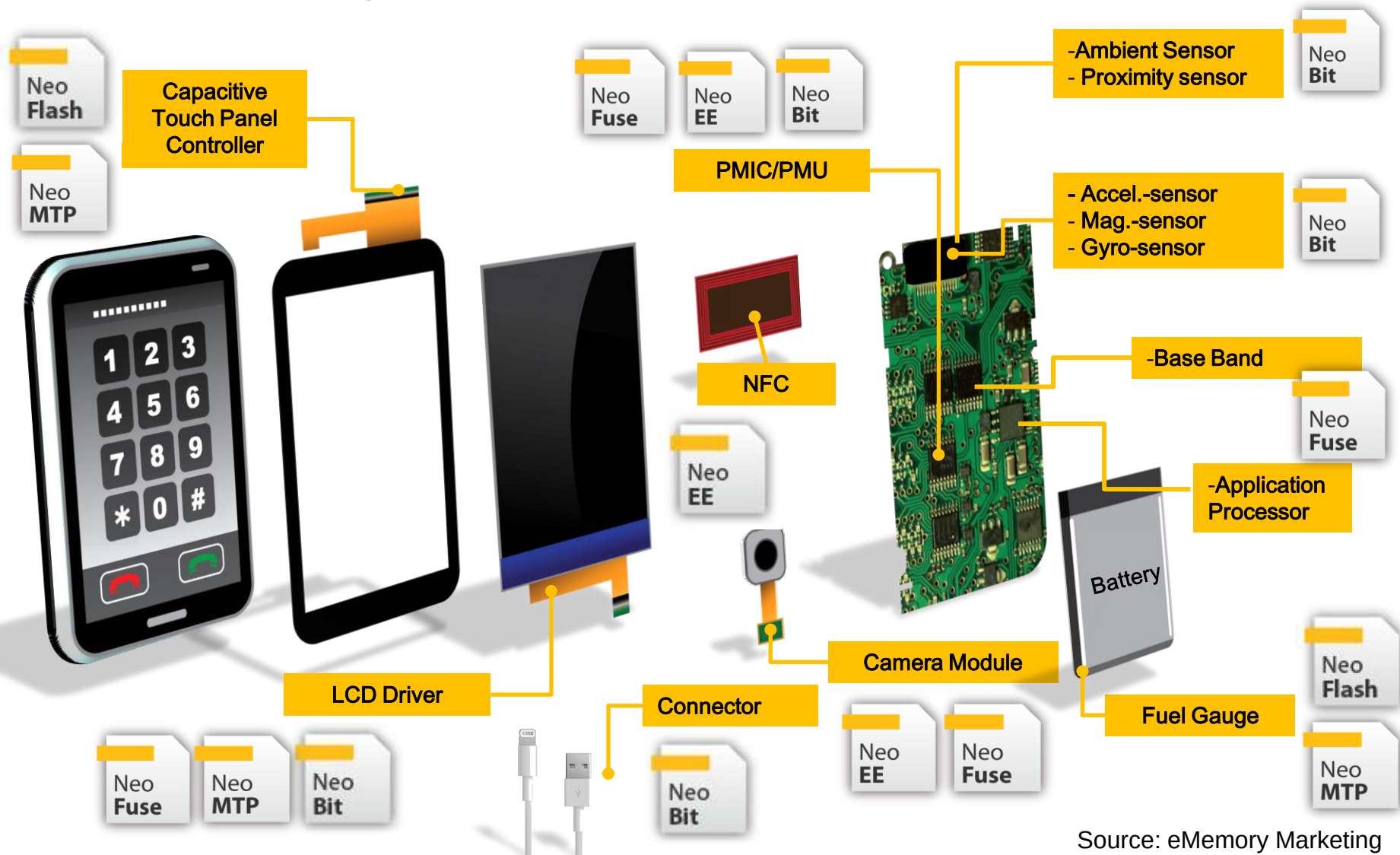
Opportunity at all Price Points

 eMemory Inside today



Note: 2.2 million 8" equivalent wafers with eMemory IP were shipped in 2013. (~5% of WW foundry shipment)

eMemory IP in Smart Phone



Source: eMemory Marketing

Benefits from Using eMemory IPs

Design-in for

1. Trimming
2. Parameter Setting
3. Code Storage
4. Identification Setting
5. Encryption
6. Function Selection

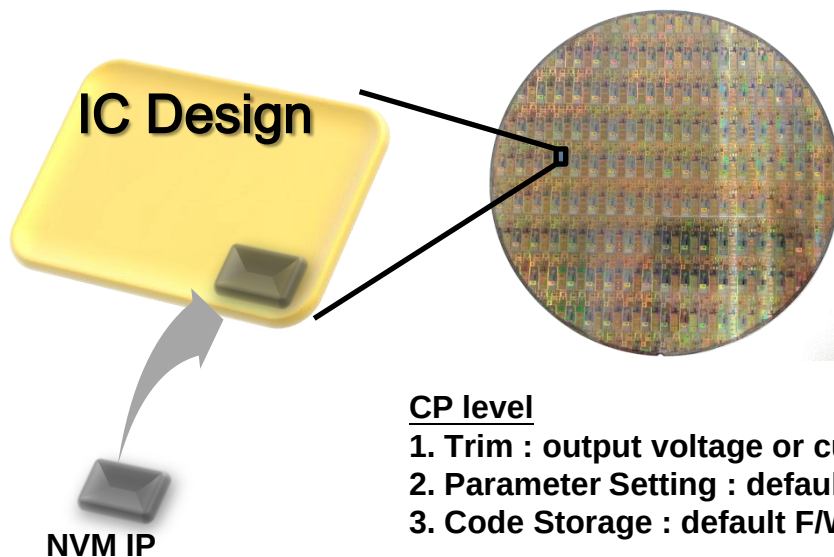
Package/FT level

1. Trim : SPEC shift
2. Parameter Setting : cross chip optimization
3. Identification Setting : manufacturer resume
4. Function Selection : setting for target market

CP Test

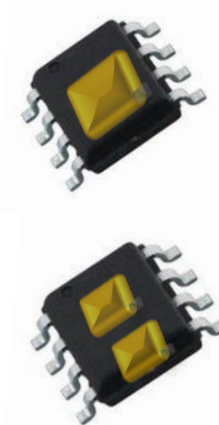
Package/FT

System Assembling



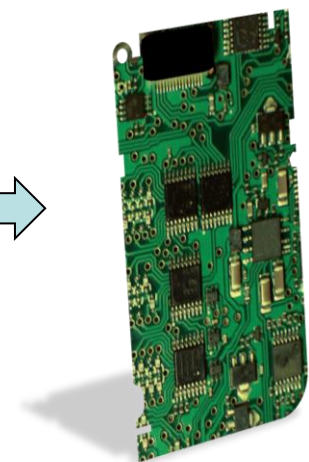
CP level

1. Trim : output voltage or current
2. Parameter Setting : default value
3. Code Storage : default F/W code



System Assembling

1. Parameter Setting : cross chip optimization
2. Code Storage : F/W code modification
3. Identification Setting : manufacturer resume
4. Encryption : Security algorithm or key storage



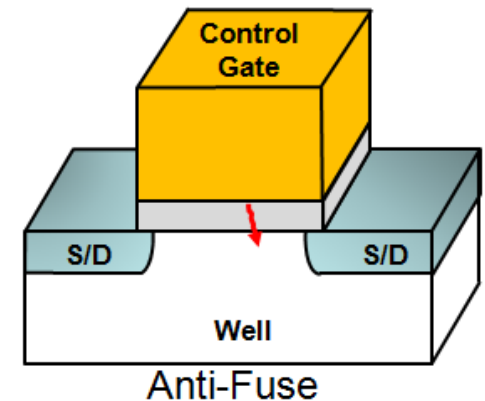
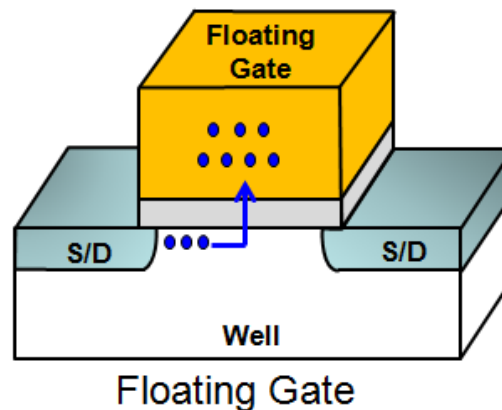
Invisibility for Security

- Provide “Invisible Hardware Key” for invisible storage
- Prevent reverse-engineering to detect content of security key
- Protect firmware and hardware of ICs from pirating
- Extend & protect customer’s business

eFuse Key: Data is easily observed



Invisible Hardware Key : Data is hard to be detected



Security & Protection

Authorized Product



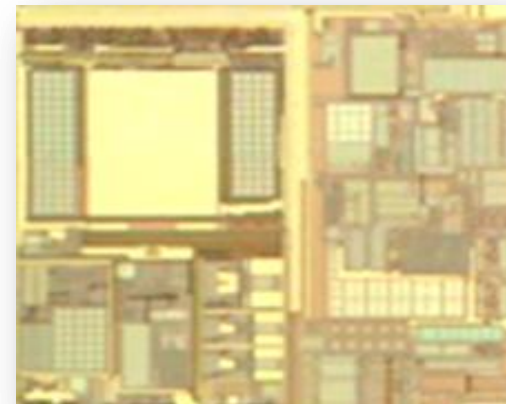
**reverse
copy**

re-produce



without protection

Fake Product

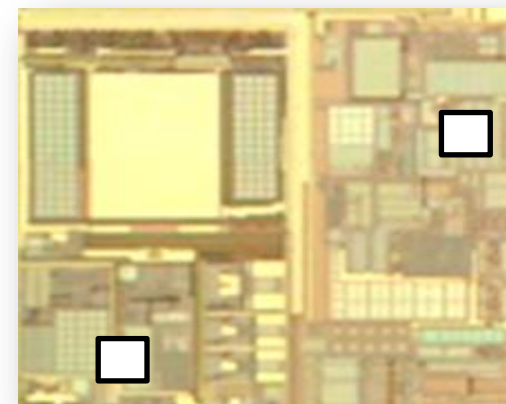


**reverse
copy**

re-produce



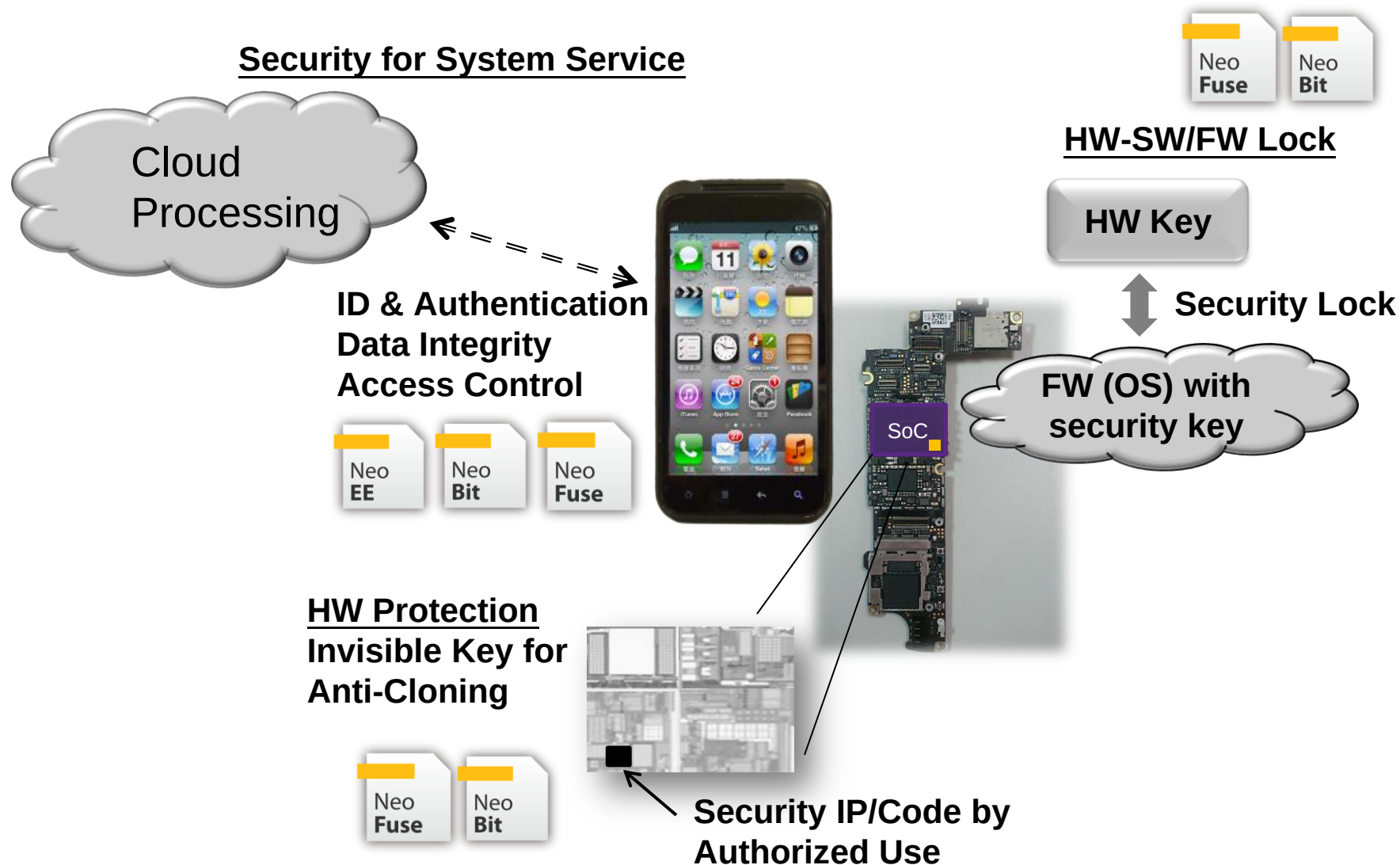
with protection



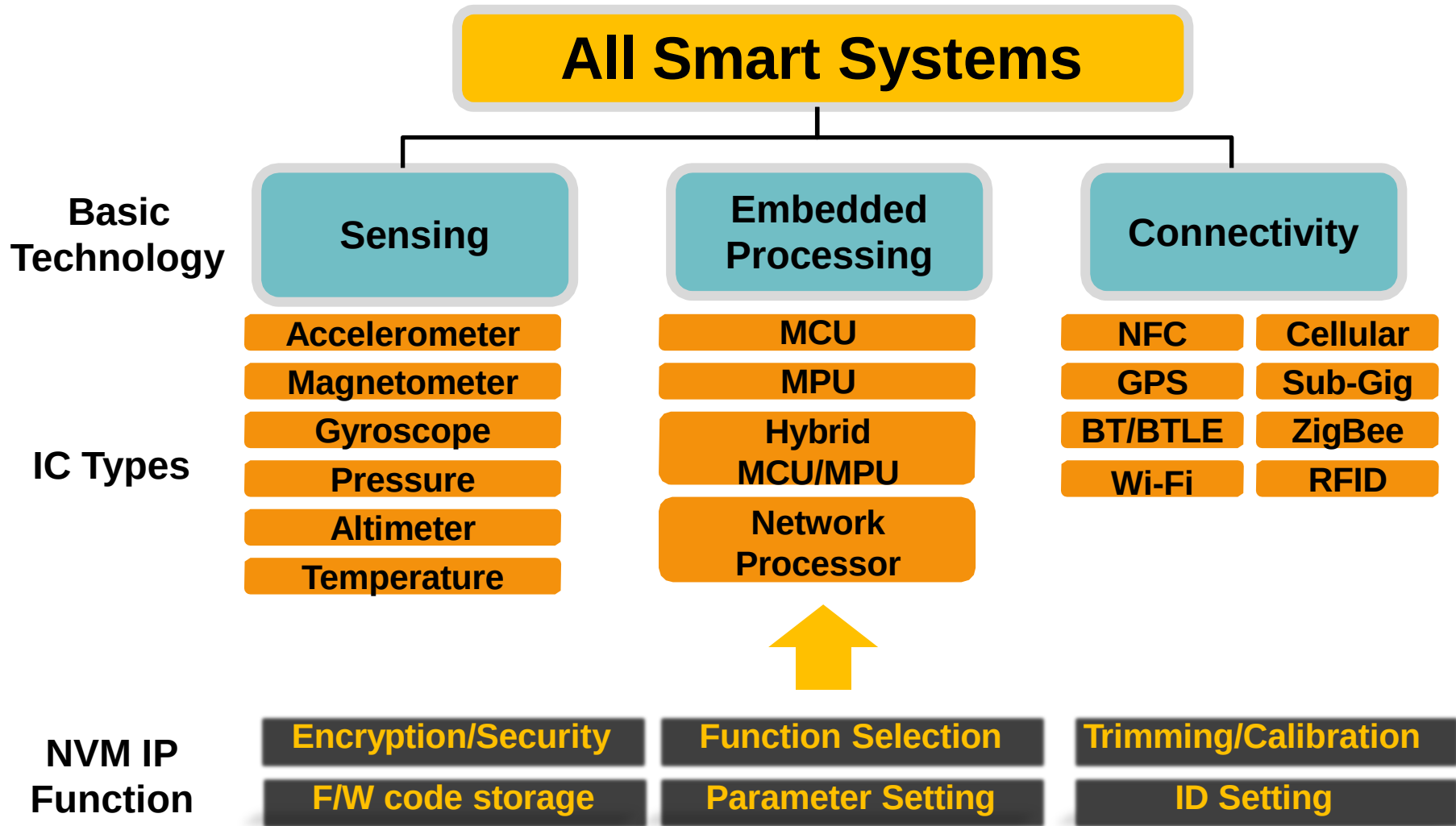
**Security IP/Code by
Authorized Use**

**Can NOT Work w/o
Security IP/Code**

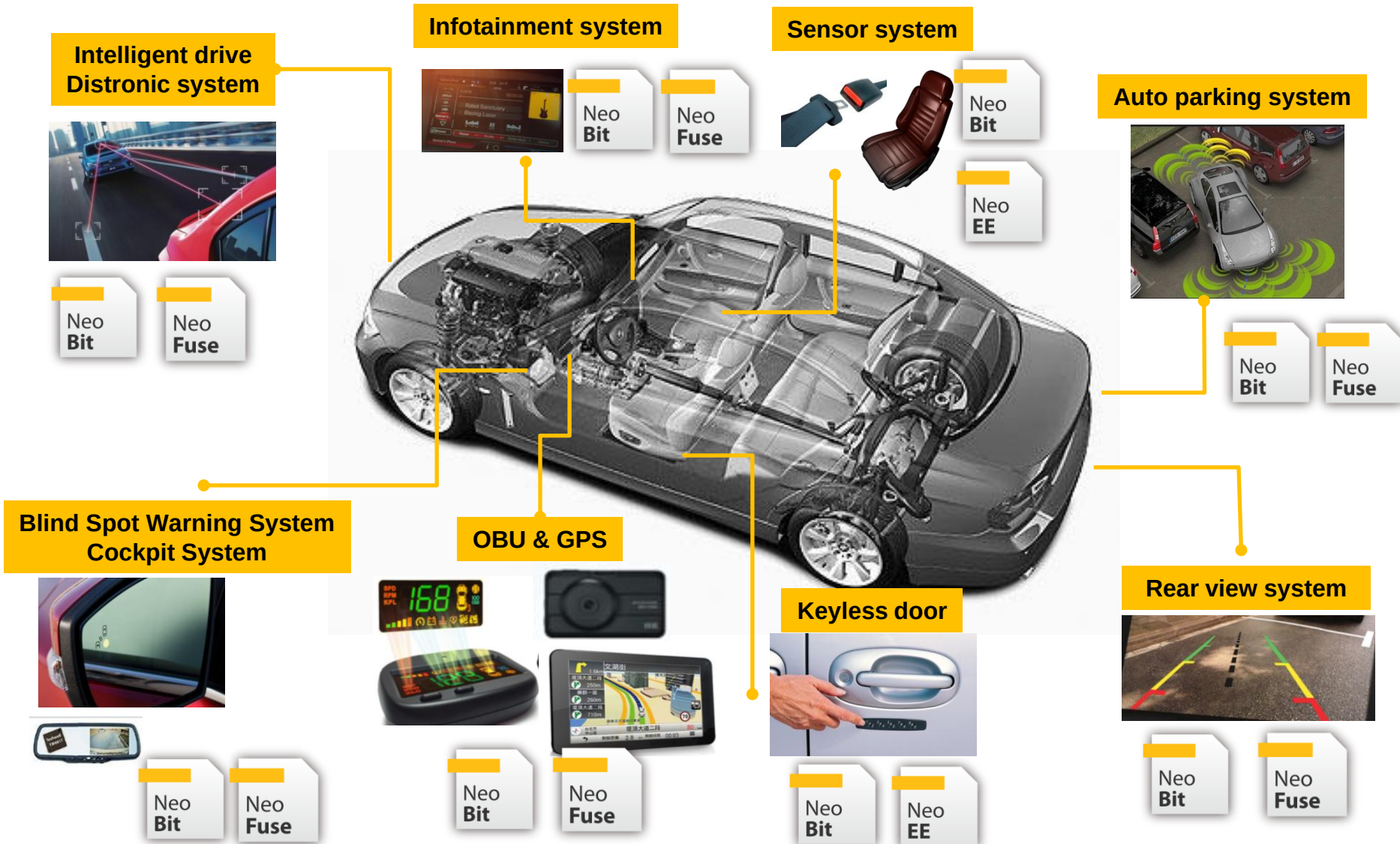
Security with eMemory IPs



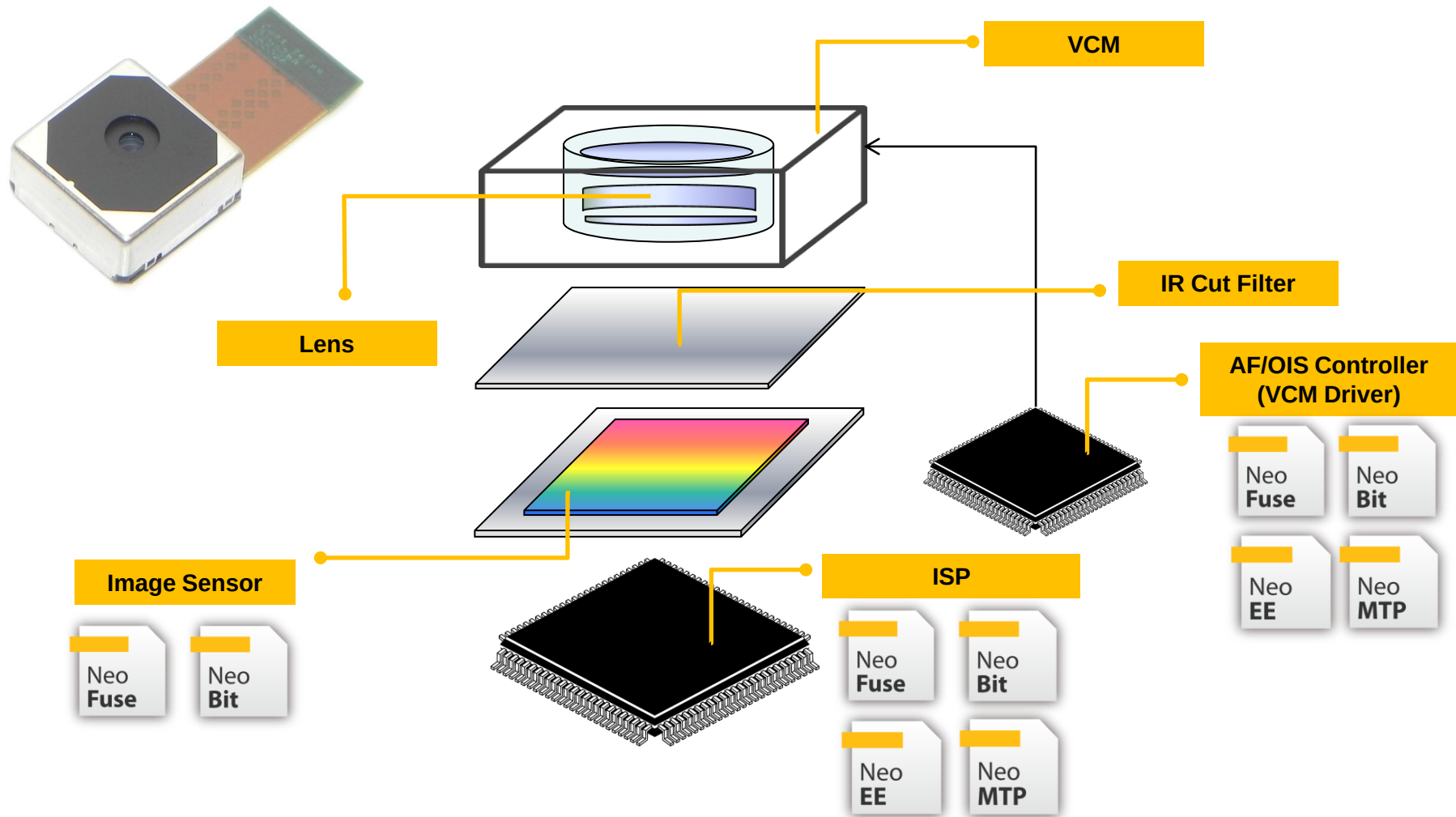
NVM IP Demand in IoT



Autotronics with eMemory IPs

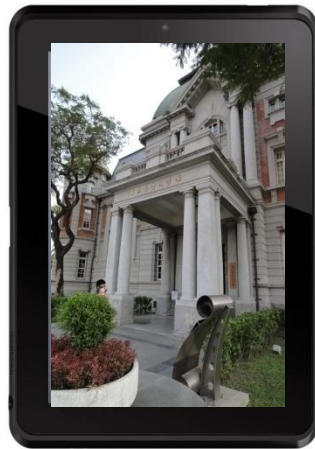


Imager Module with eMemory IPs



Advanced LCD Driver ICs

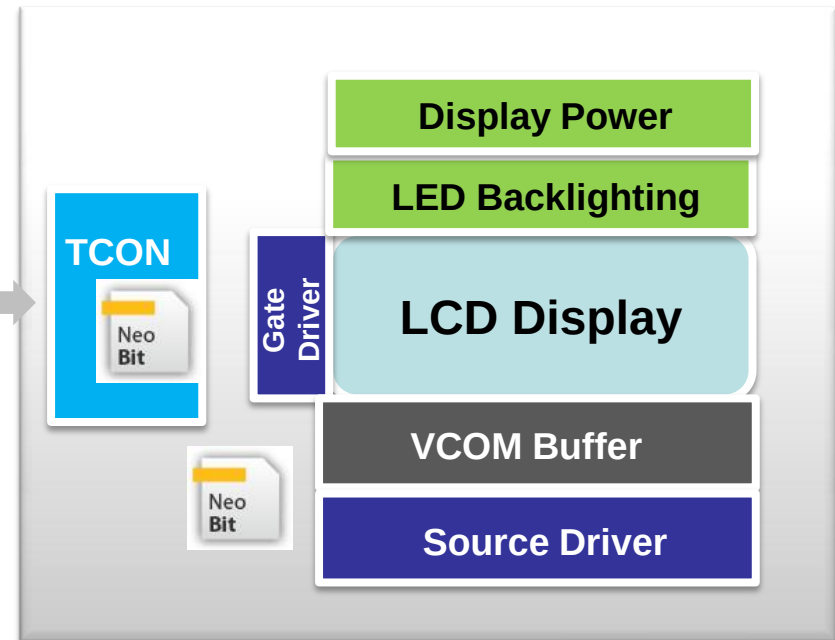
Process Technology : 0.11um HV/80nm HV/55nm HV



I/F
(LVDS, MIPI,...)



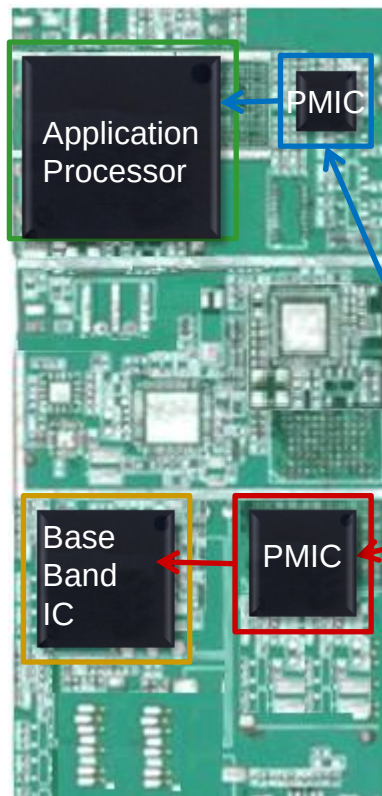
DDI



Density	Endurance	NVM Type	Purpose	NVM Usage
2K8~4K8	1	OTP	Trimming	1. Accuracy enhancement 2. Mismatch cancellation
			Code Storage	1. Gamma Correction Table 2. Timing Control Pattern 3. Color Engine Enhancement

Power Management ICs for Baseband and Application Processor

Process Technology : Advanced 0.25um BCD/ 0.18um BCD/ 0.13um BCD
Mature 0.18um/0.16um/0.152um Logic

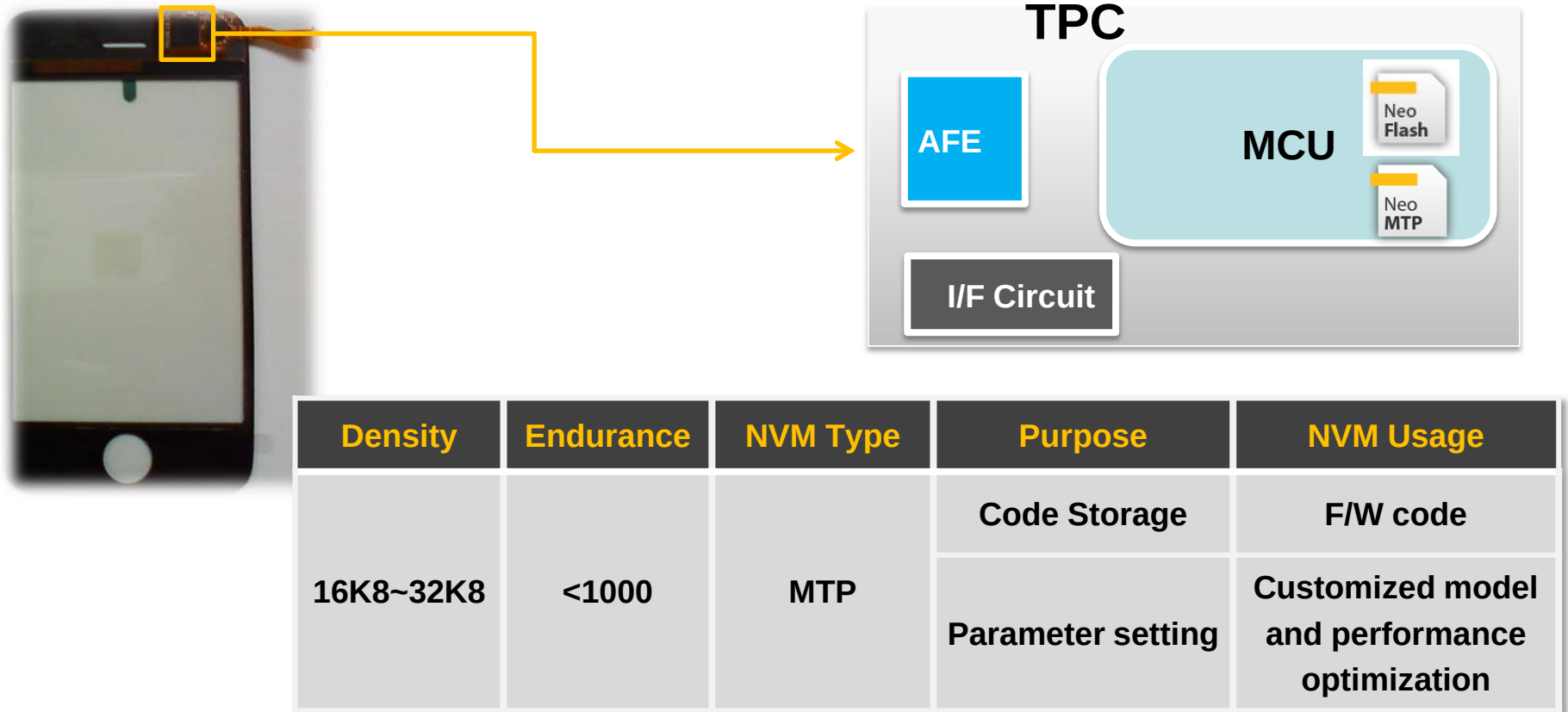


Density	NVM Type	Purpose	NVM Usage
2Kb~4Kb	OTP	Trimming	DC/DC, Bandgap
		Parameter Setting	Design flexibility & Performance optimization
		Code Storage	Start-up behavior & smart power saving algorithm



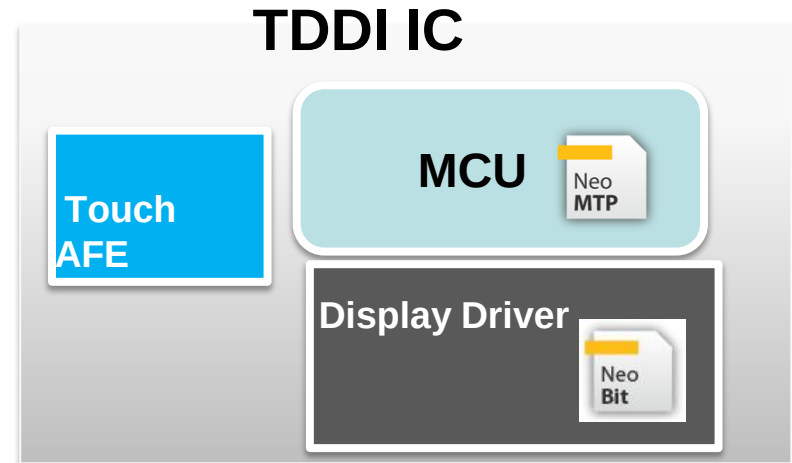
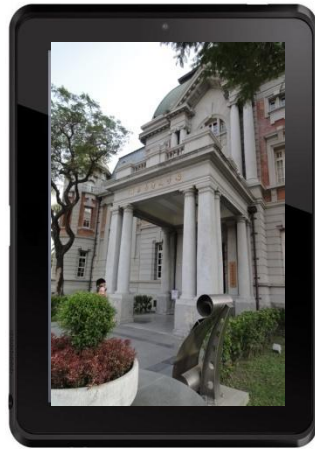
Touch Panel Controller ICs

Process Technology : 0.16um HV/0.11um G



In-Cell Touch Panel Controllers ICs

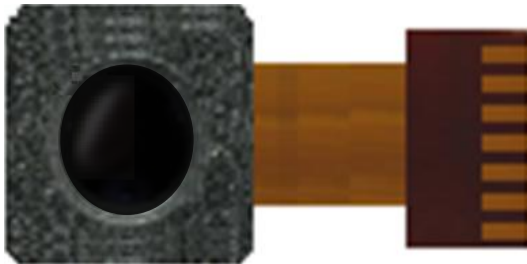
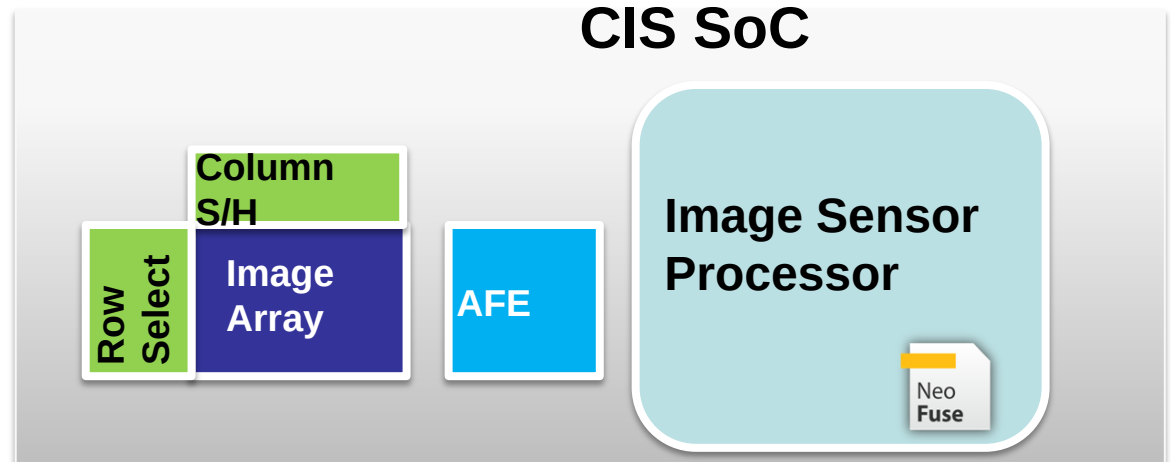
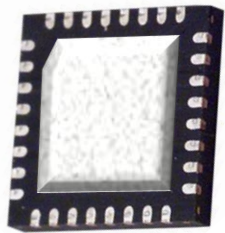
Process Technology : 0.11um HV/80nm HV/55nm HV



Density	Endurance	NVM Type	Purpose	NVM Usage
2K8~4K8	1	OTP	Trimming	Accuracy
			Code Storage	Gamma Table
16K8~32K8	<1000	MTP	Code Storage	Touch F/W Code
			Parameter setting	Performance Optimization

CMOS Image Sensor

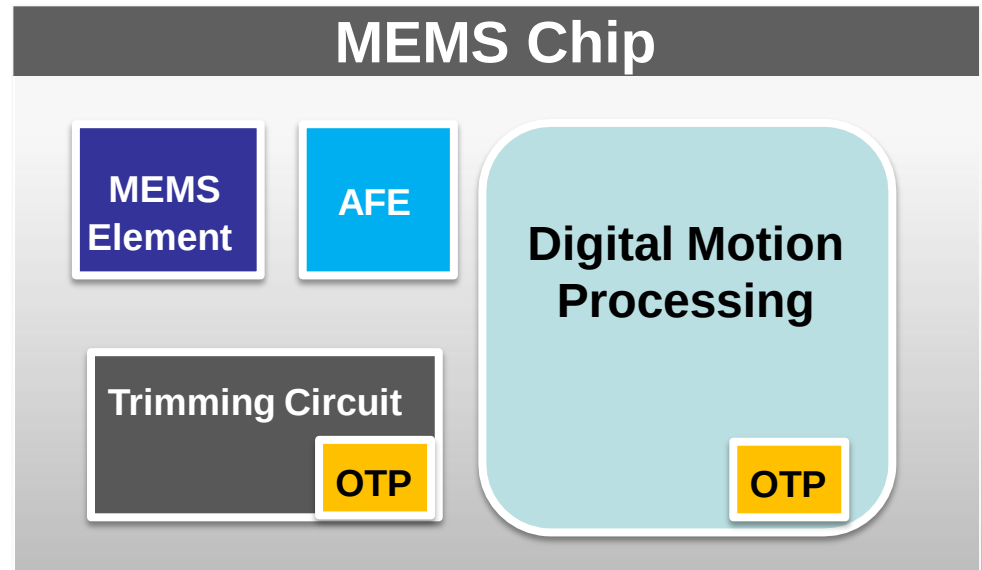
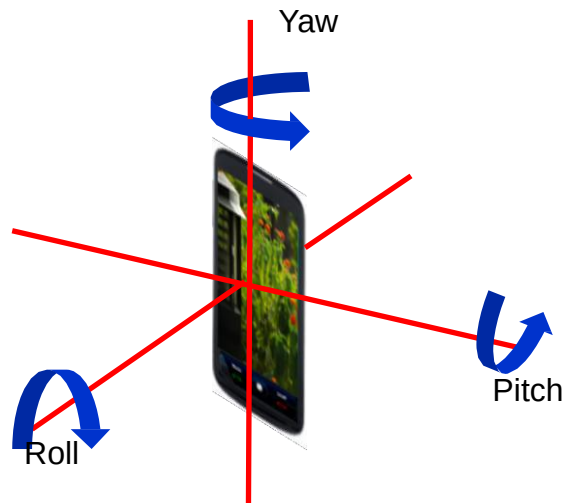
Process Technology : 0.11um CIS/90nm CIS/65nm CIS



Density	Endurance	NVM Type	Purpose	NVM Usage
2Kb~4Kb	1	OTP	Identification Setting	Product Code
			Parameter Setting	Start-up Initial Setting
32K8	1	OTP/ROM	Code Storage	Boot Load

MEMS

180/160/15x nm HV/Logic for MEMS Controller

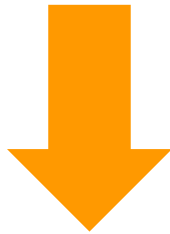


Density	NVM Type	Purpose	NVM Usage
2Kb~4Kb	OTP	Trimming	Factory trimming
		Parameter Setting	Signal filtering
		Code Storage	Geometric computation

Replacement of Embedded Flash for Competitiveness Improvement

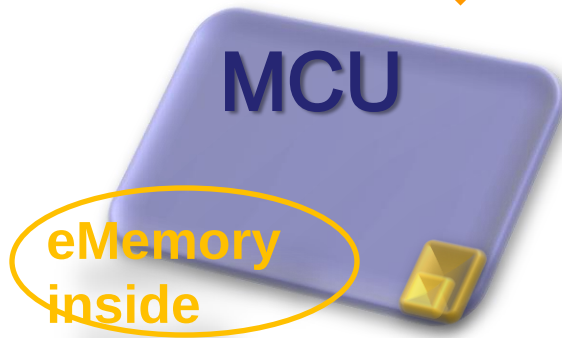


product design & manufacturing by
embedded Flash
Logic Process + 10 Masks



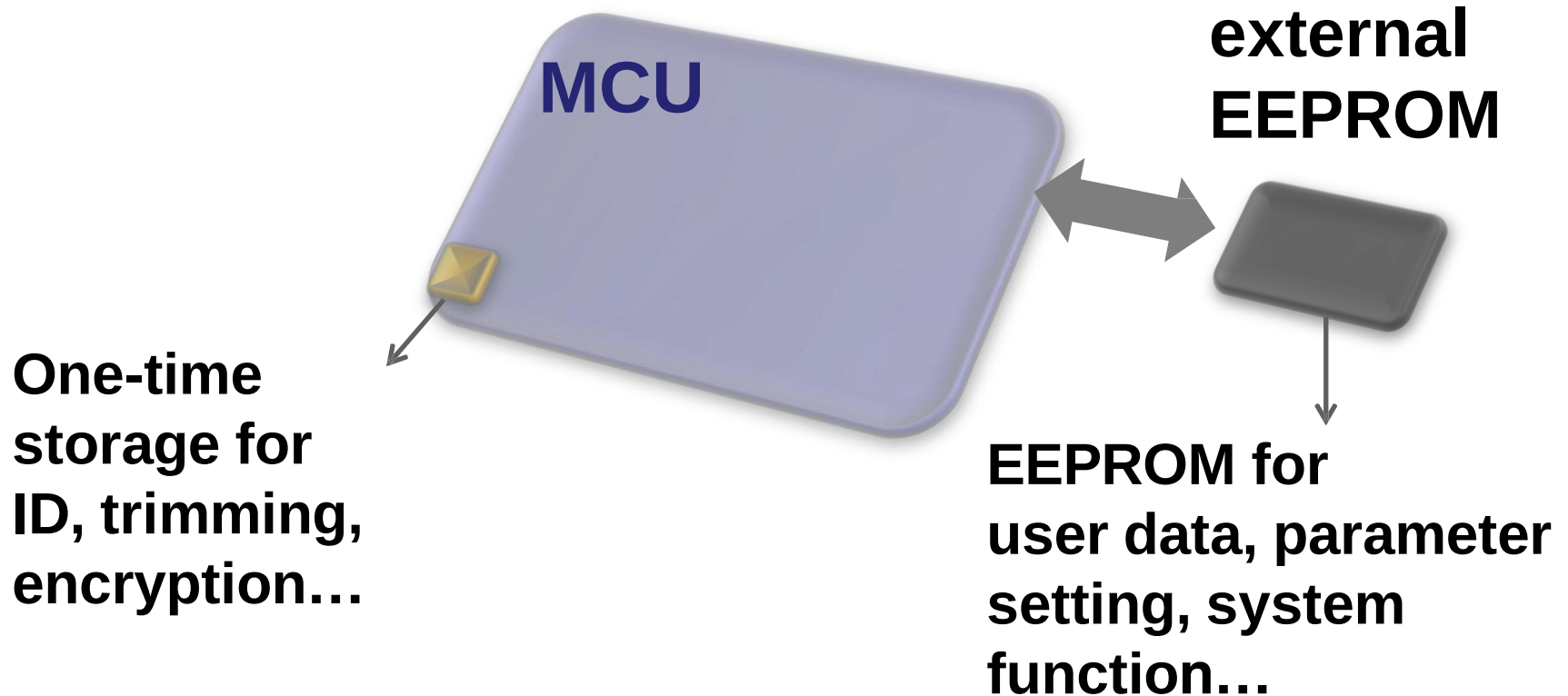
***30% more
cost reduction***

***wafer cost &
testing time***



product design & manufacturing by
Embedded Logic NVM (OTP/MTP)
Logic Process

MCU Applications with EEPROM



NeoBit + NeoEE

Hybrid NVM solution (NeoBit + NeoEE) with customized SPEC & optimized size



- **One single IP by integration of NeoBit & NeoEE**
- **Help for system size reduction**

Wafer Demand by IC Type

IC Type	Equ. to 8-inch wafer (K)
AP	4964
PMU	4756
CIS sensor	4226
Fingerprint	4000
Smart card controller	3000
Base Band	2935
LCD driver (with TCON)	2013
Gauge IC	627
Touch panel controller (C)	556
Connectivity	395
STB controller	335
TV controller	327
Wifi controller	245
LED driver	243
DC-DC/AC-DC	176
Accelerator sensor controller	124
Light snesor	121
Bluetooth controller	121
Gyroscope sensor controller	104
TAG IC	76
DVD controller	67
MCU (8bits, LV/3.3V)	56
MCU (8bits, LV/3.3V)	56
P-Gamma	52
MCU (8bits, pure 5V)	51
NB CAM controller	42
Pressure sensor controller	20
Touch pad controller	18
PC CAM controller	15
Touch panel controller (R)	5
TCON (w/o driver)	4

2014.8.29 updated

Outlook for 3Q and Beyond

- Applications in major smart phone customer continue their momentum and expand to wearable devices.
- PMICs in Chinese smart phone continue to increase production and expand to new power management applications , such as fast charger and wireless charger.
- TDDI and 55nm LCD Drivers start to ramp up.
- Applications in STB, Fingerprints, and CIS will ramp up in 2H of 2015.
- Due to security requirement and yield issue, replacement of e-fuse by NeoFuse is accelerating in the advanced process nodes.
- Co-work with leading foundry and European auto-electronic customers to provide automotive grade IP.

Key Growth Drivers

Growth in value per mobile devices

- More chip applications per smartphone/tablet product.

Growth into more markets

- From consumer electronics and mobile devices to wearable devices.
- Adding new NVM product lines further enable more product applications.

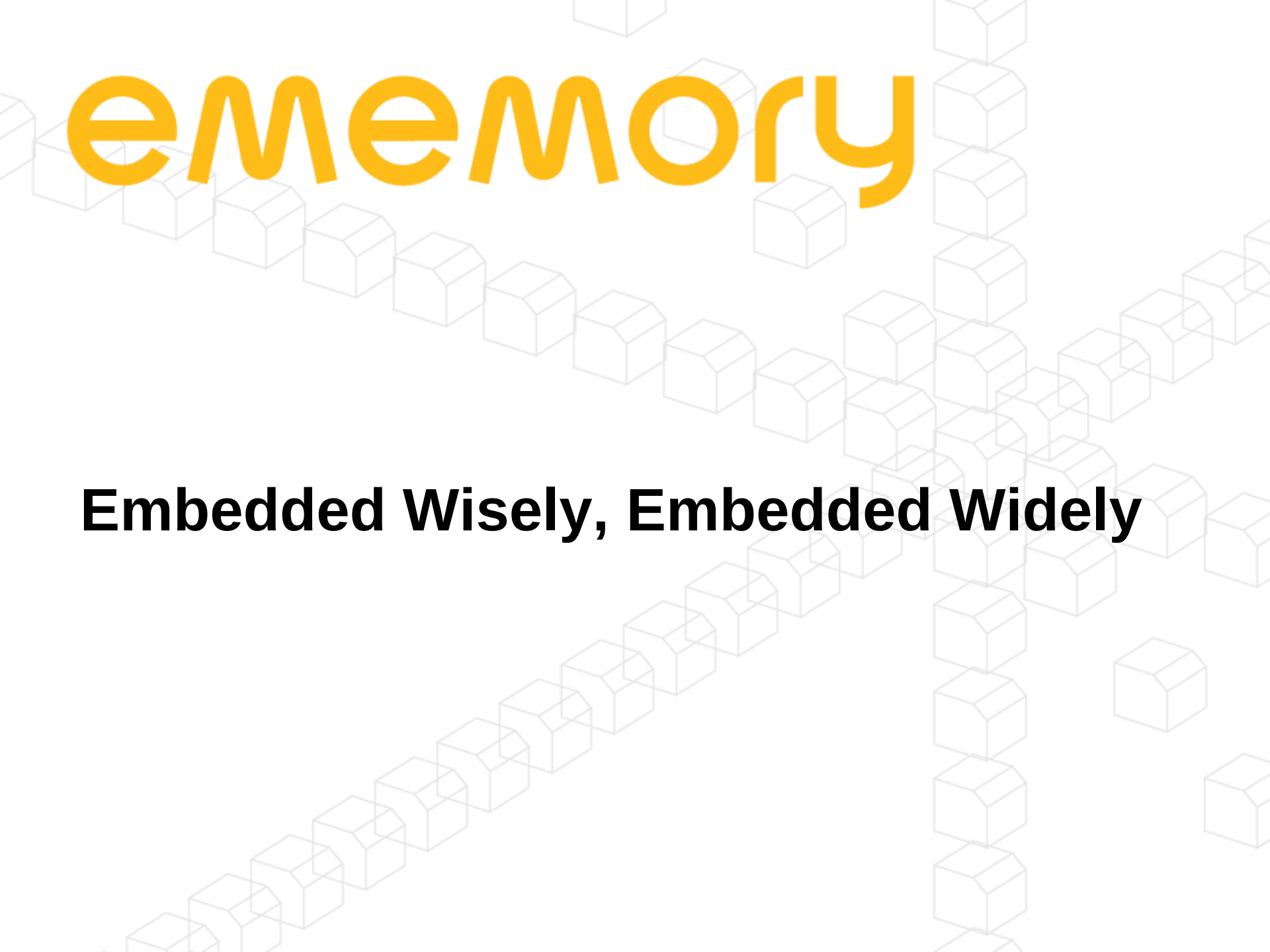
Growth in more advanced technology

- Higher royalty per wafer is contributed from more advanced technology nodes.

IoT great era

- Embedded Logic NVM will be a must.

Q & A



ememory

Embedded Wisely, Embedded Widely