

The background of the slide is a light gray color with a pattern of 3D cubes. The cubes are arranged in a way that creates a sense of depth and perspective, with some cubes appearing to be stacked or overlapping. The cubes are rendered in a simple, wireframe style with light gray outlines.

eMemory

MTP Technology Seminar

Jan. 14th, 2015

IPR Notice

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Outline

- **MTP Market Applications and Strategy**
- **MTP Technology Introduction**

Outline

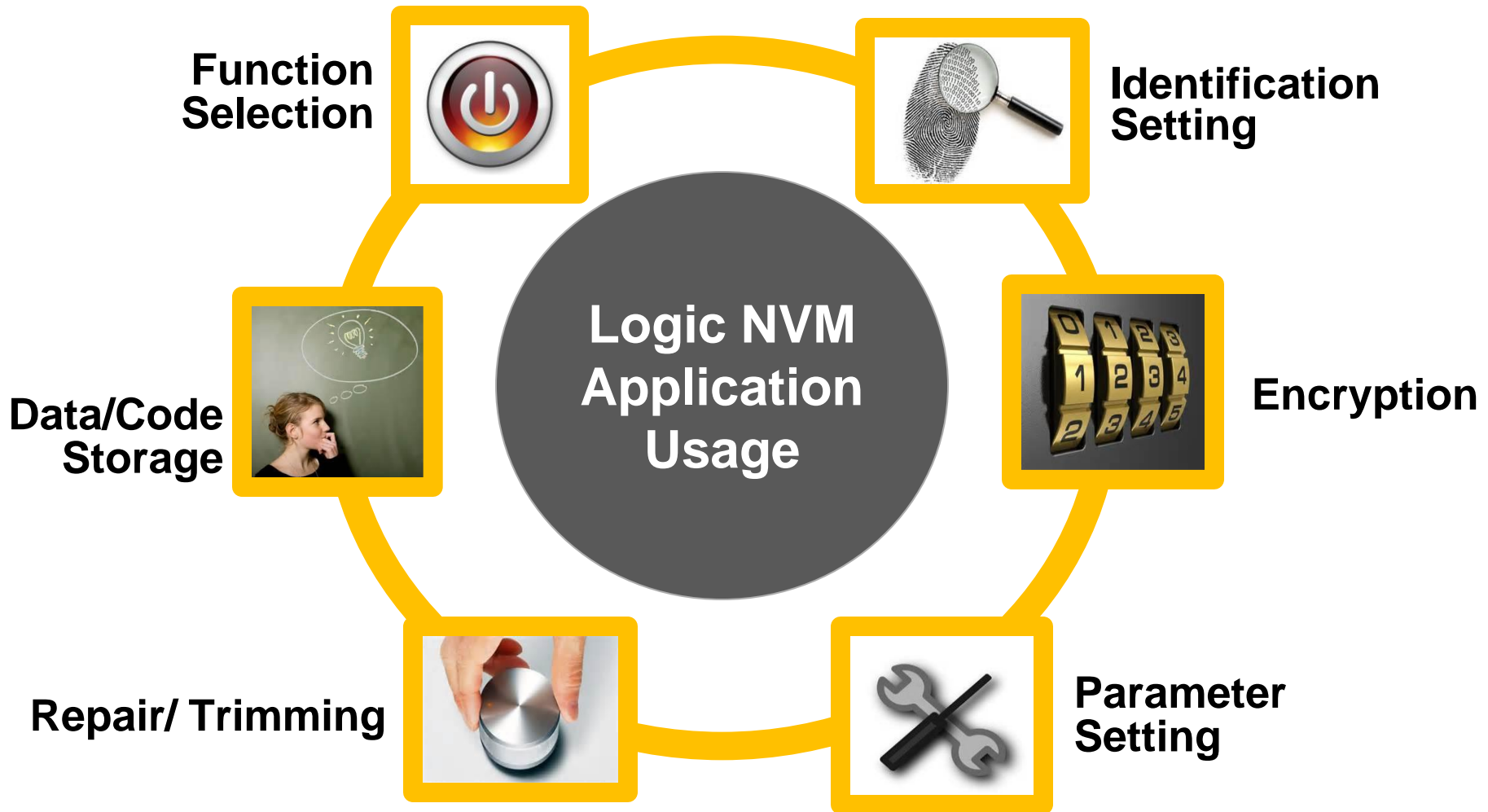
- **MTP Market Applications and Strategy**
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eMemory Logic NVM

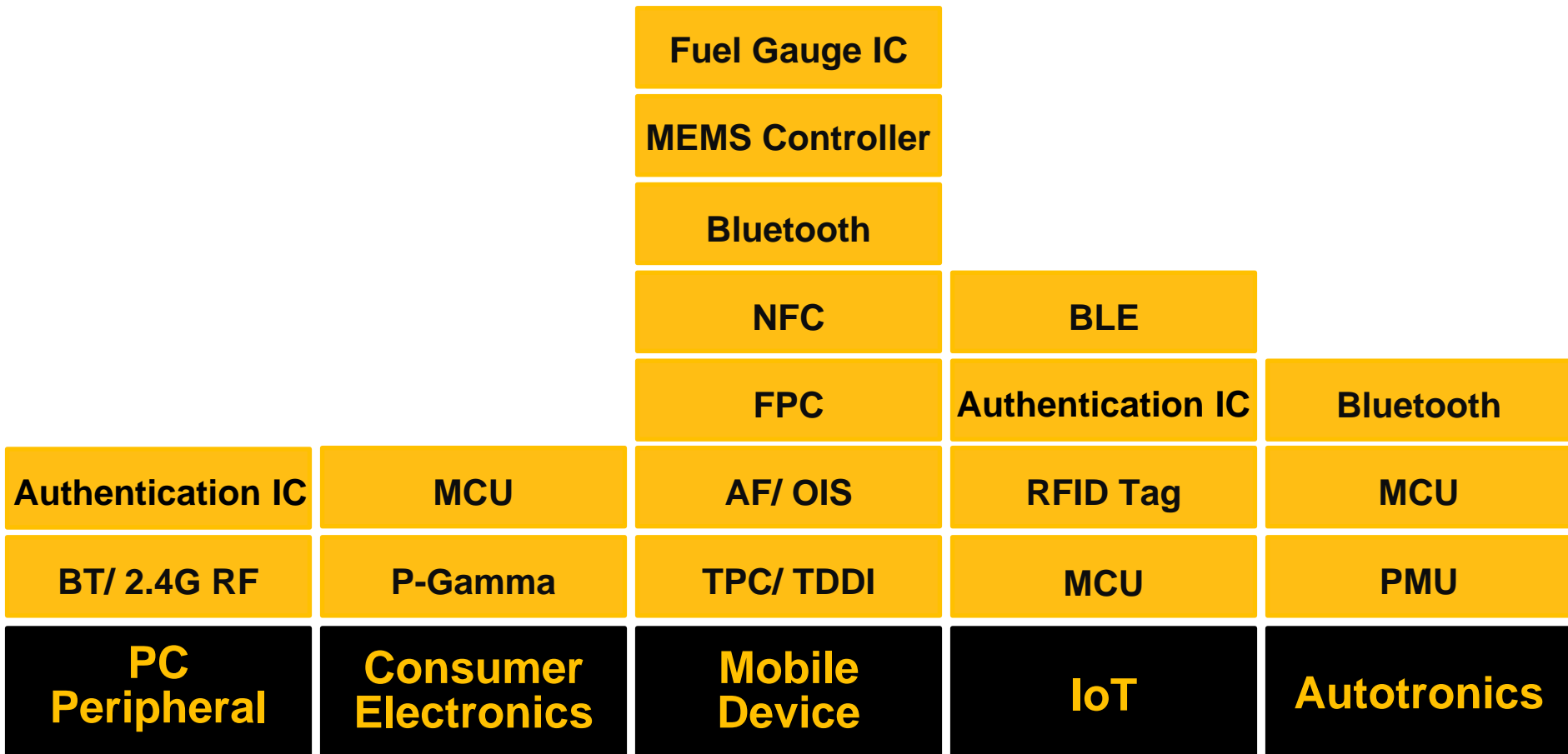
- › Compatible to any process
- › Robust reliability
- › Low process cost
- › Competitive IP sizes
- › Easy integration
- › Easy porting

eMemory Logic NVM	OTP		MTP	
	NeoBit	NeoFuse	NeoEE	NeoMTP
Product Type	OTP	OTP	EEPROM	MTP
Endurance (Cycles)	10	10	10K~100K	1K~10K
Additional Mask	0	0	0	0
Technology	Floating gate	Anti-Fuse	Floating gate	Floating gate
Scalability	Simple	Simple	Simple	Simple
Memory Density	HD < 512Kb GHD < 16Mb	< 4Mb	< 4Kb	< 512Kb
Testability	Yes	No	Yes	Yes

Logic NVM Usages



MTP Applications



eMemory Strength

- **Complete Logic NVM Portfolio**
 - › OTP, MTP, Flash and EE
- **Production Track Record**
 - › Over 2800 product usages
 - › Over 10Million production wafers (>>20B IC chips)
- **Wide customer base**
 - › Over 800 fabless customers bring up with latest market demands,
 - › Strategic alliance with 18 foundries enables new product applications.

Strategy for Technology Development

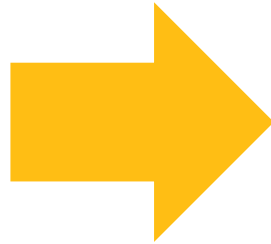
- **High Portability Helps Customers' Migration**
 - › Easy porting from one process node to another,
 - › Easy porting from one foundry to the other.
- **Guaranteed High Yield and Reliability**
 - › Reliable for data storage,
 - › Stable with high production yield.
- **Low Cost Solutions**
 - › No mask adder ,
 - › Low production cost from wafer manufacturing to product testing.

Strategy for MTP Process Development

- Process migration toward advanced nodes

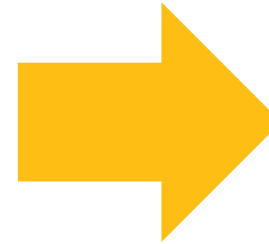
NOW

**MP @
0.3um,
0.18um,
0.16um,
0.153um,
0.11um**



2015/E

**More MP @
80nm HV
55nm HV,
40nm LP,**



2016/M

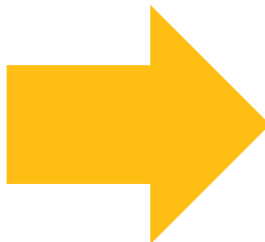
**More MP @
40nm HV
28nm
16nm**

Strategy for MTP IP Development

- IP performance enhancement for low-power/
high reliability application.

NOW

- **Consumer-Grade**
- **Industrial-Grade**



2015/E

- **Ultra-low power**
- **Automotive/Autotronics**

Strategy for Business Development

- Hybrid solutions offering to help system size reduction.

External EEPROM in MCU application

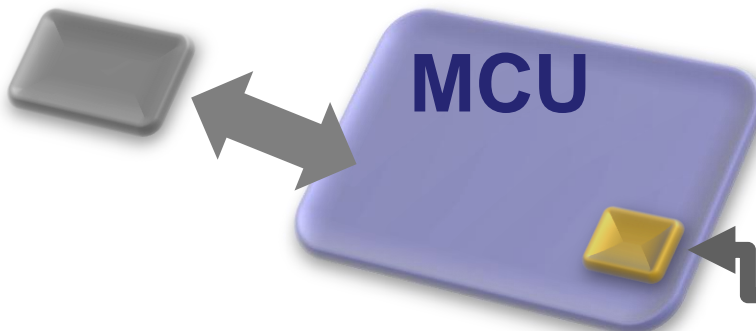
for user data, parameter setting, system function...

PC Peripheral	Consumer Electronics
Autotronics	IoT



IP with NeoBit + NeoEE

External EEPROM



OTP for ID, trimming, encryption...

Strategy for Business Development

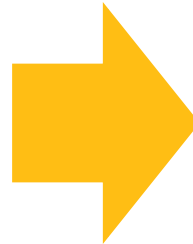
- Hybrid solutions improve customers' profitability.

MTP for system-level optimization

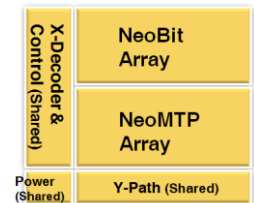
IoT	Autotronics	Mobile Device
BLE MCU	Bluetooth MCU	Fuel Gauge IC Bluetooth TPC
Consumer Electronics	PC Peripheral	
MCU	BT/ 2.4G RF	



30% Cost Reduction



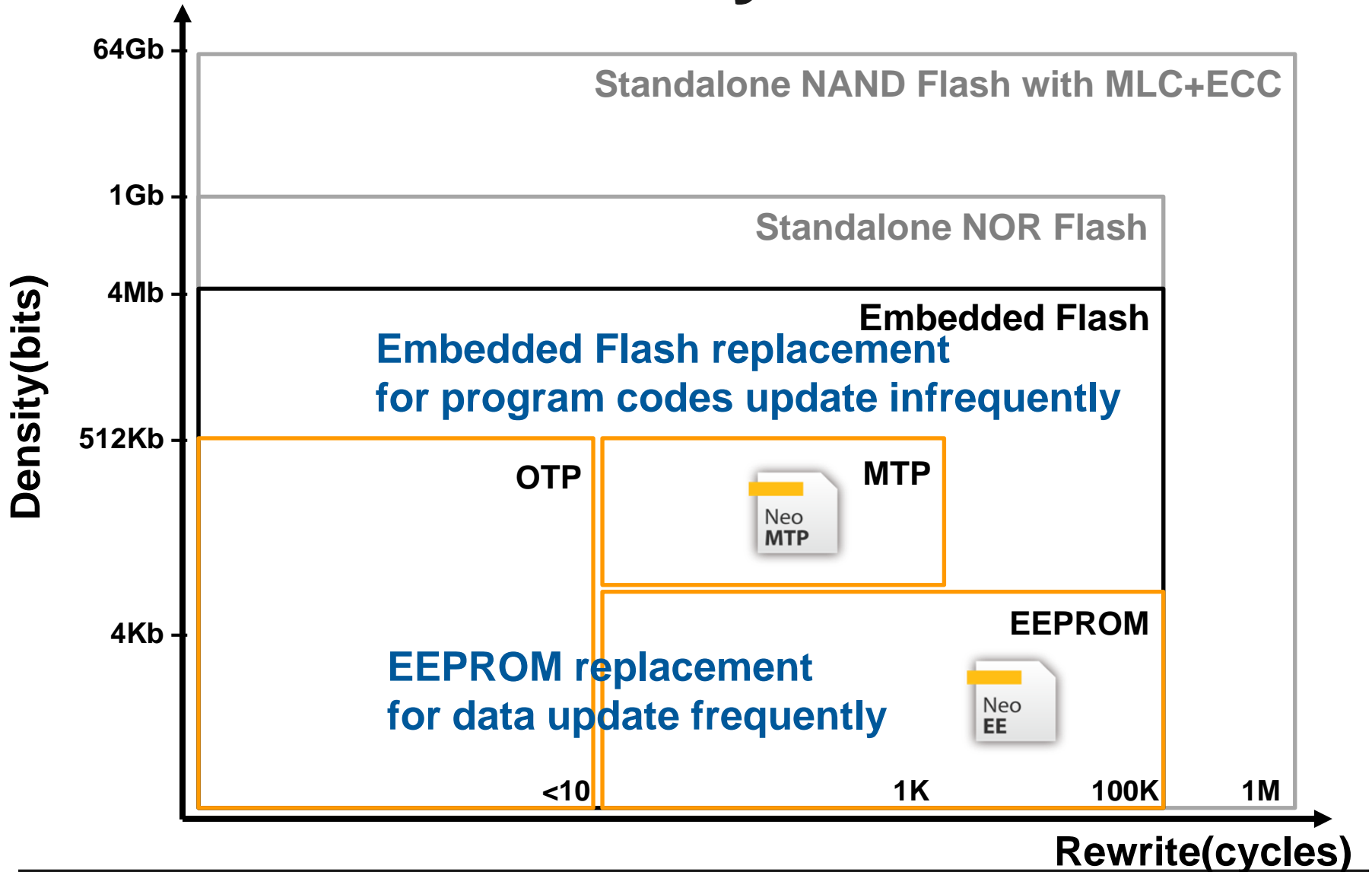
+ 40% Cost Reduction



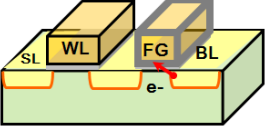
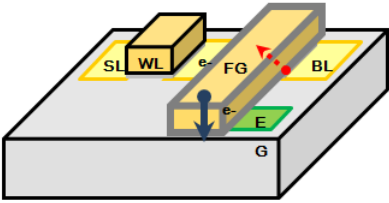
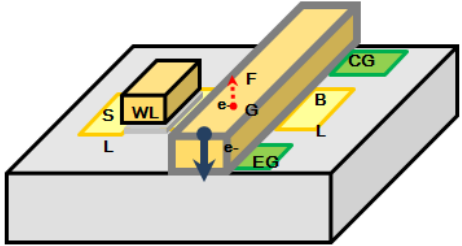
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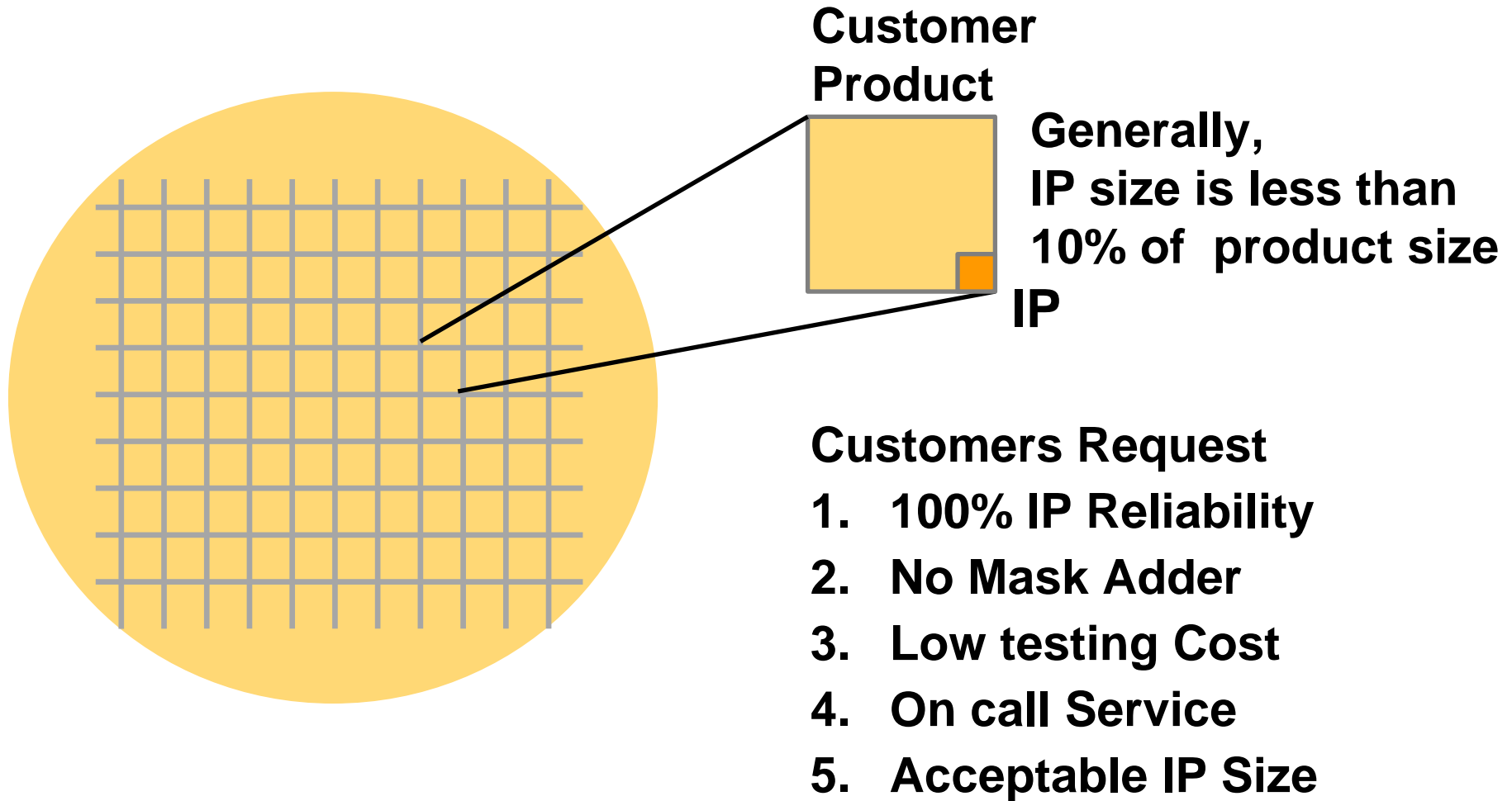
Nonvolatile Memory Classifications



eMemory FG Technology Family

eMemory's NVM Technology	OTP	MTP	
	NeoBit	NeoMTP	NeoEE
Process Demand	CMOS Compatible Process with +0 extra mask		
Memory Base	3.3V or 5V IO Device		
Program Scheme	CHE	CHE	FN
Erase Scheme	UV	FN	FN
Cell Structure			

Considerations for IP Adoption



Yield and Reliability Matter

- **High product yield helps lower product cost**
 - › testing coverage vs. product yield
- **High reliability makes sure system application function well with long lifetime**
 - › reliability vs. yield overkill

**Customer Biz competitiveness comes from
100% product yield with 100% reliability coverage**

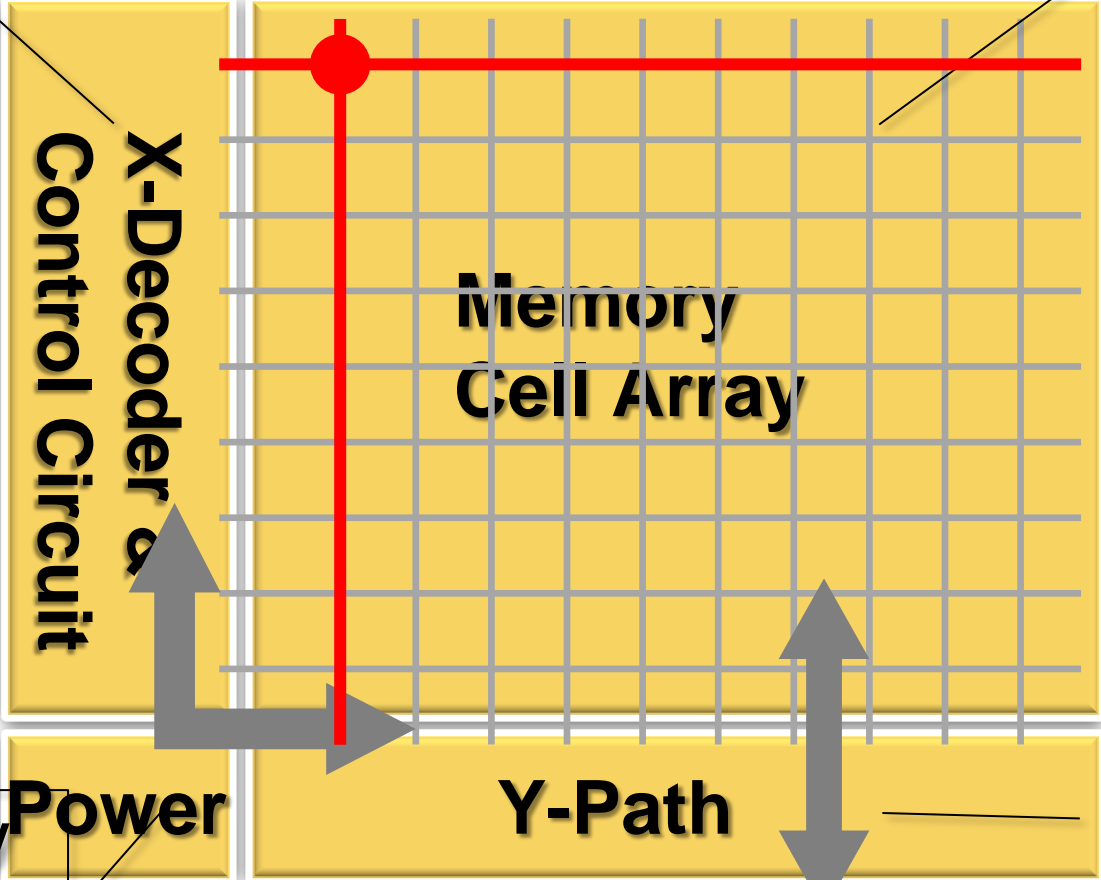
Needs for MTP with +0 Extra Mask

- **Fast product/technology development.**
- **Easy cross FAB porting for production planning.**
- **Short process cycle time for fast time to market.**
- **Competitive wafer/process cost.**

Inside Nonvolatile Memory IP

Program,
Erase and
Read
operation
control

Where data
is stored.
Each cross
point has a
memory cell.



Power supply
for operations

Data input &
output

High Density MTP vs. Low Density MTP

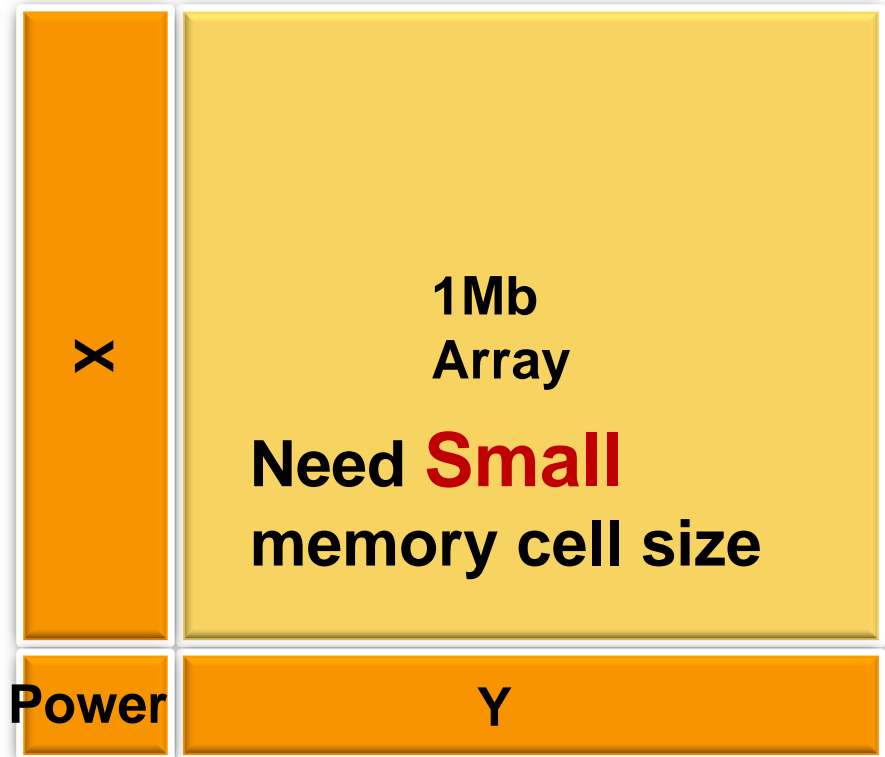
Memory Array contributes most of IP size >80%

Peripheral Circuit

contributes most of IP size >80%



Need **Simple, Scalable** peripheral design



NeoMTP: Embedded Flash Replacement

- **Target Segment:**

- › **Medium Density (<512Kb), Multiple Rewrite Cycles (up to 1K)**

- **Strength:**

- › **MTP IP similar to OTP IP size**

- › **100% yield with high reliability demonstrated on eMemory FG common platform**

- › **Competitive testing with 100% reliability coverage**

NeoEE: EEPROM Replacement

- **Target Segment:**

- › Low Density (<4Kb), High Rewrite Cycles (up to 100K)

- **Strength:**

- › Ultra compact IP size, scalable with density
- › 100% yield with high reliability demonstrated on eMemory FG common platform
- › Ultra low power operating (<10uA) for 10yr lifetime
- › High temp. operation (125C/150C) for Autotronics

eMemory's MTP

- **Evolve from eMemory's OTP with 10M Wafers Production Record.**
- **0 Mask Adder.**
- **2T Structure Facilitates Simple Control Logic and Reduces Testing Cost.**
- **Competitive IP Size**
- **Extend Business into Embedded Flash and EEPROM Applications.**

**How to Provide 100% *Yield* and *Reliable*
MTP in the Chip with 0 Mask Adder is
Quite a Challenge !**

“We have proved we can do it !”

eMemory

The background of the slide is filled with a pattern of 3D cubes. Some cubes are solid white, while others are outlined in light gray. They are arranged in various orientations and positions, creating a sense of depth and a grid-like structure.

Embedded Wisely, Embedded Widely