The background of the slide is filled with a pattern of white, 3D wireframe cubes. These cubes are arranged in various orientations and positions, creating a sense of depth and movement. Some cubes are in the foreground, appearing larger and more detailed, while others are in the background, appearing smaller and more faded. The overall effect is a modern, geometric aesthetic.

# eMemory

## **A Leading Logic NVM Company**

**May, 2015**

# IPR Notice

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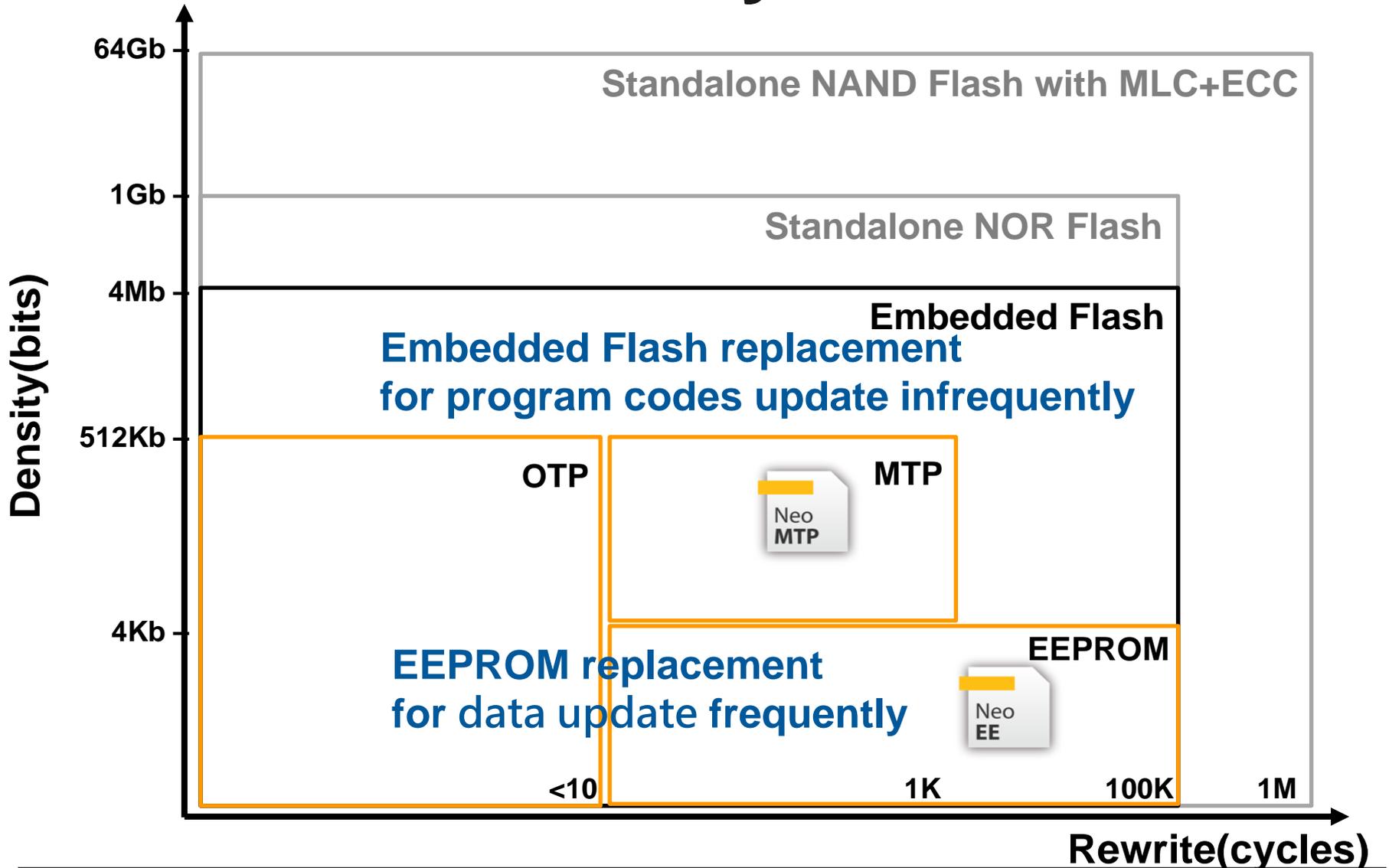
# Cautionary Statement

**This presentation contains forward-looking statements, which are subject to risk factors associated with semiconductor and intellectual property business. It is believed that the expectations reflected in these statements are reasonable. But they may be affected by a variety of variables, many of which are beyond our control. These variables could cause actual results or trends to differ materially and include, but are not limited to : wafer price fluctuation, actual demand, rapid technology change, delays or failures of customers' tape outs into wafer production, our ability to negotiate, monitor and enforce agreements for the determination and payment of royalties, any bug or fault in our technology which leads to significant damage to our technology and reputation, actual or potential litigation, semiconductor industry cycle and general economic conditions. Except as required by law, eMemory undertakes no obligation to update or revise any forward-looking statements, whether as a result of new information, future events, or otherwise.**

# Outline

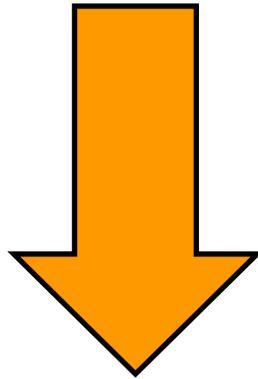
- **Business Model**
- **Review of Operations**
- **Growth Opportunity and Future Outlook**
- **Q & A**

# Nonvolatile Memory Classifications



# What's Logic Non-Volatile Memory (NVM)

**Embedded NVM = LOGIC + 10 Masks**



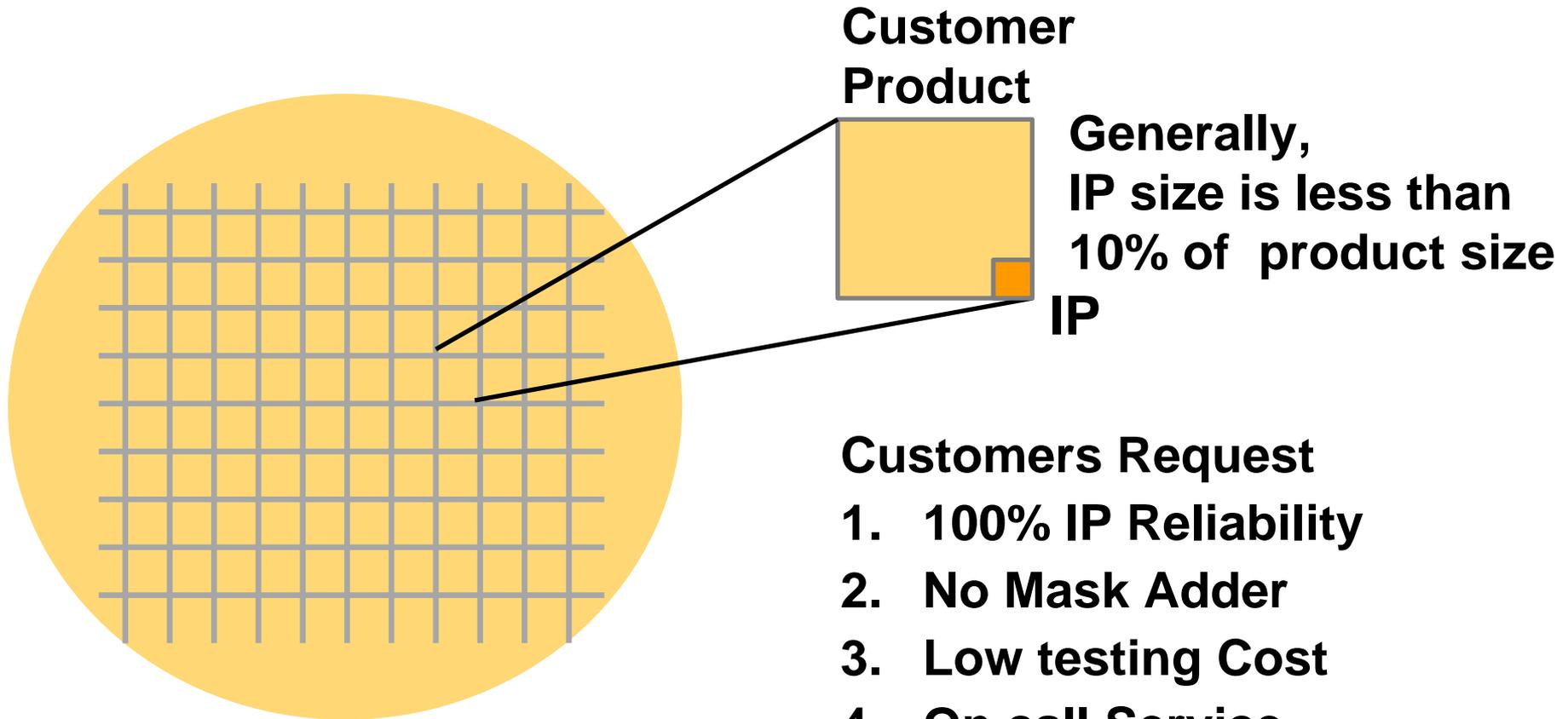
*30% more  
cost reduction*

**Embedded LOGIC NVM = LOGIC**

# Embedded NVM Technologies

	ROM	eFuse (OTP)	Antifuse (OTP)	CMOS Floating Gate (OTP)	CMOS Floating Gate (MTP)	Embedded Flash
Cell Structure	Transistor	Poly Fuse	Antifuse	Floating Gate	Floating Gate	Floating Gate
Standard CMOS Compatible	Yes	Yes	Yes	Yes	Yes	No
Bitcell Area	< 1	50	1	2	4	1
Endurance	No	No	< 10	< 10	10K-100K	100-1000K
Density	4Kb-1Mb	256bit-4Kb	16bit-1Mb	16Kb-1Mb	1Kb-2M	64Kb-4Mb
Security	Low	Low	High	High	High	High
Additional Steps	None	None	None	None	None	+10 Mask

# Considerations for IP Adoption

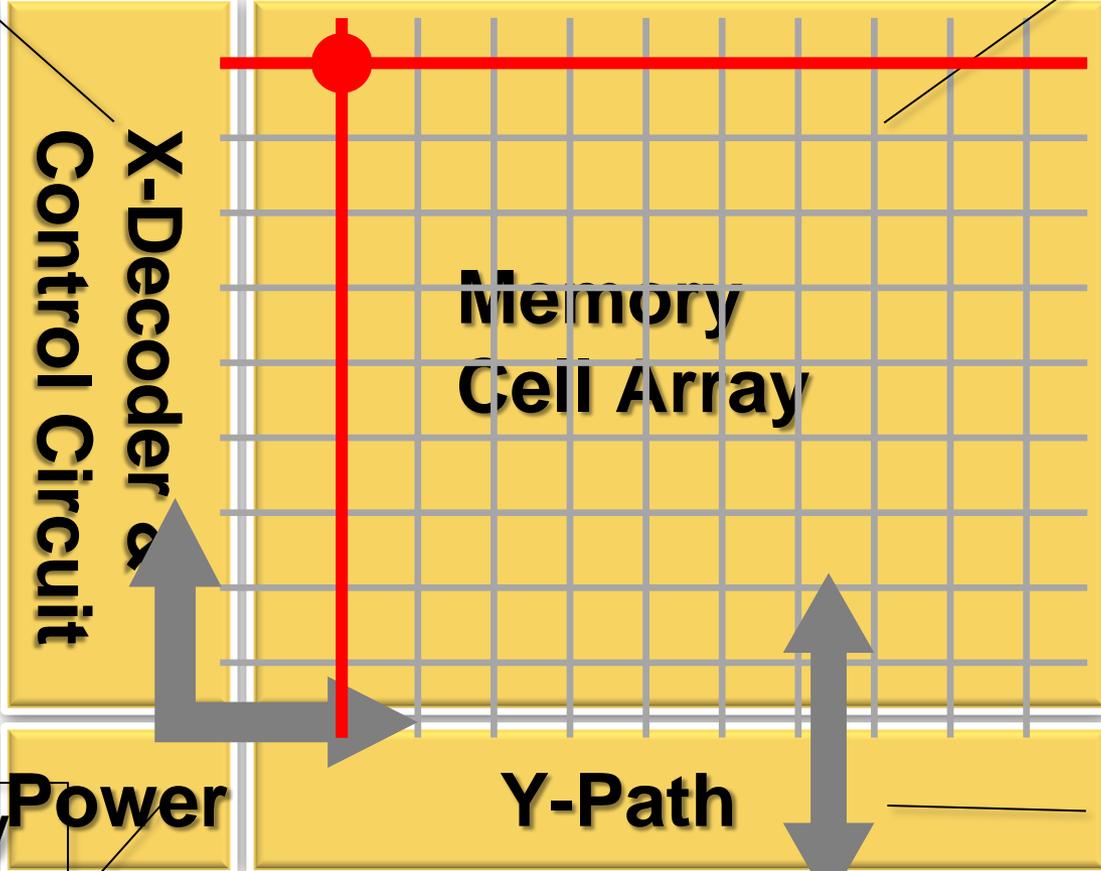


## Customers Request

1. 100% IP Reliability
2. No Mask Adder
3. Low testing Cost
4. On call Service
5. Acceptable IP Size

# Inside Nonvolatile Memory IP

Program,  
Erase and  
Read  
operation  
control



Where data  
is stored.  
Each cross  
point has a  
memory cell.

Power supply  
for operations

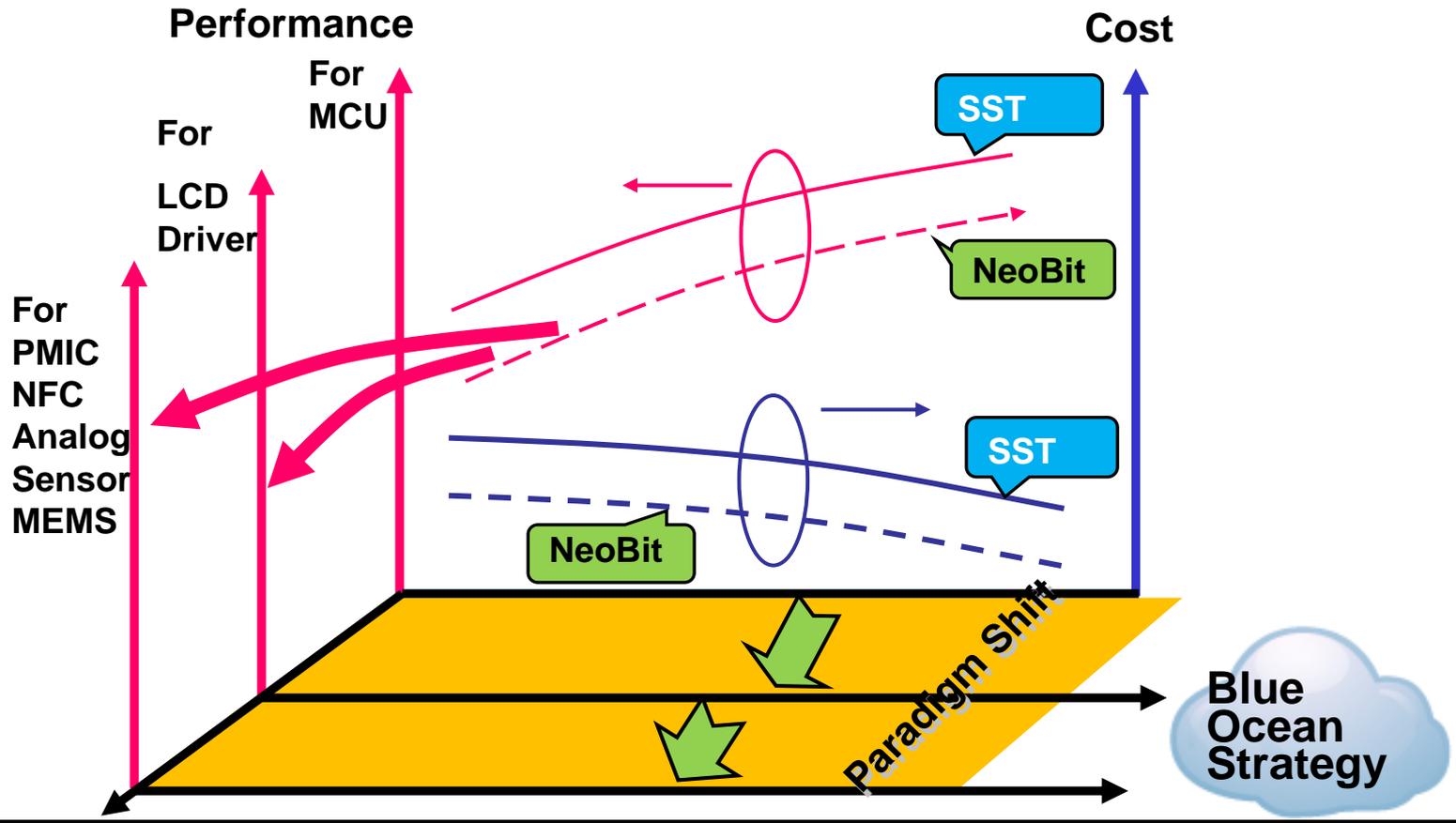
Power

Y-Path

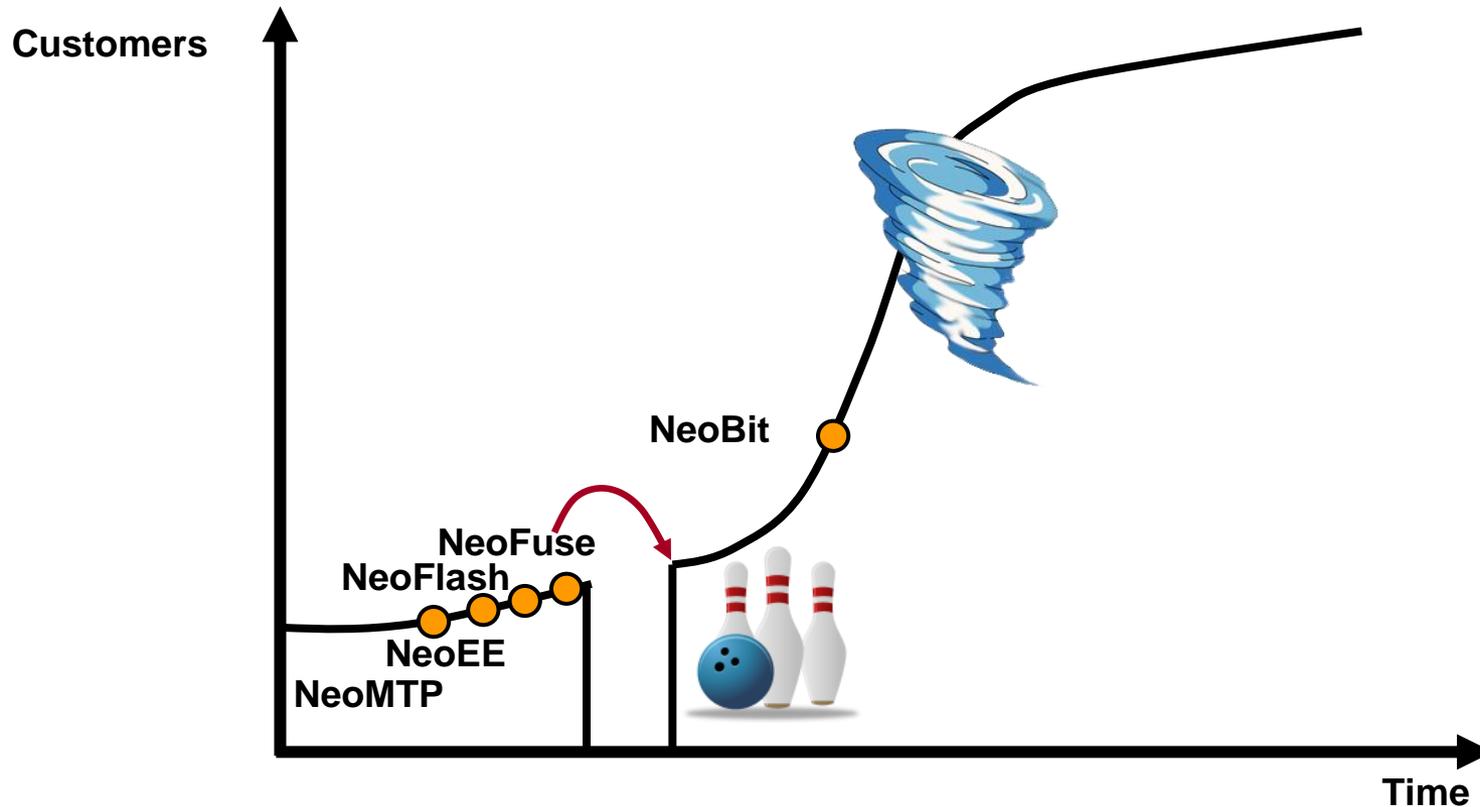
Data input &  
output

# What We Have Done

● *Innovation, Innovation, and Innovation !*



# Crossing the Chasm



# Business Model

- Founded in 2000. First customer engaged in 2002. Achieved profitability in 2005 and IPO in 2011. The largest logic non-volatile memory IP company, 210 employees (142 R&D).
- Since its IPO, the company initiated no new fund raising or bank debt, and has distributed in excess of 100% of earnings in cash dividends.
- **Growth Indices:** 1) No. of on-going technology platforms  
2) No. of design licenses  
3) Royalty



# Worldwide Customers



## Foundry



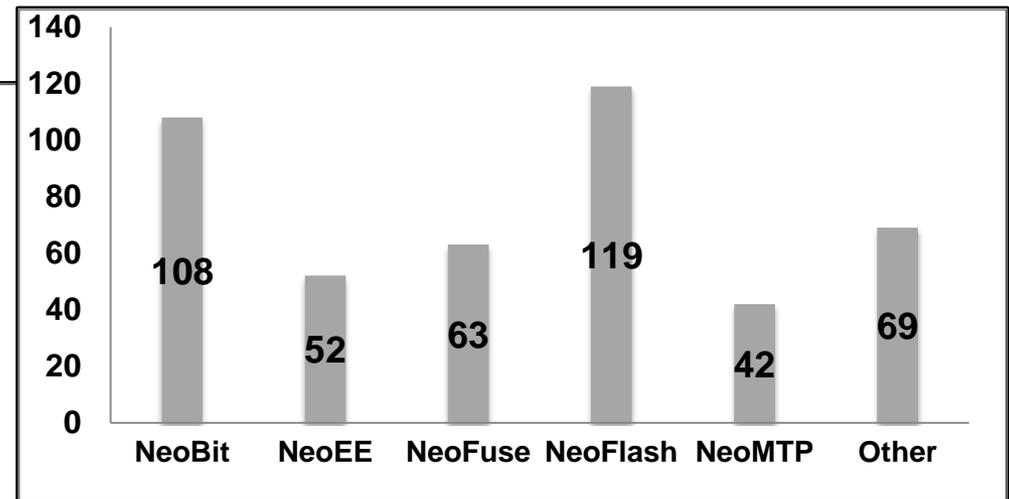
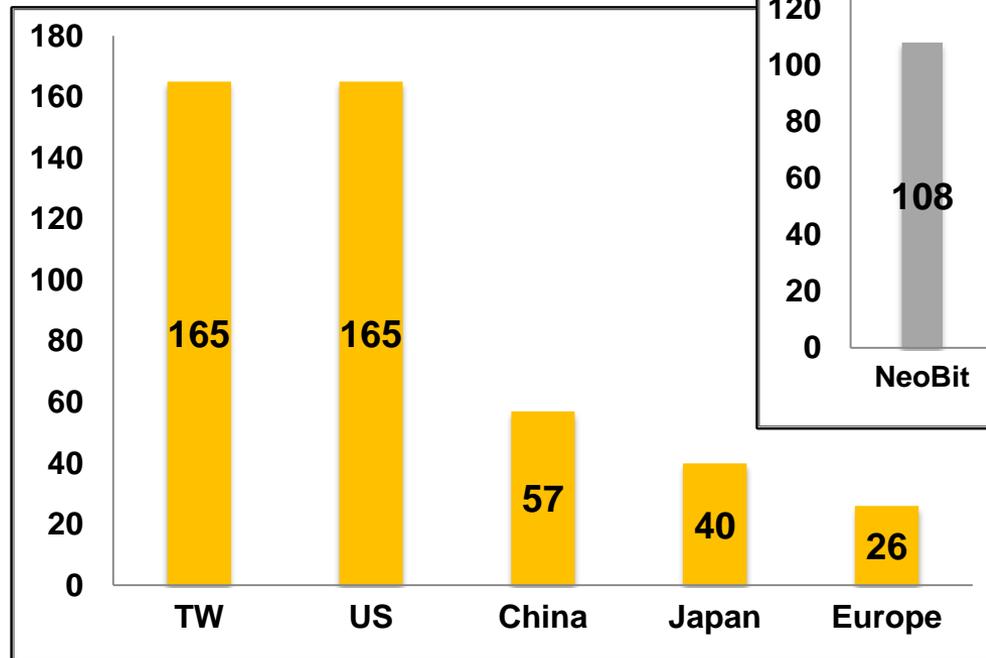
## IDM



	Taiwan	China	Korea	Japan	North America	Europe	Others
Foundry	5	6	3	2	1	0	1
IDM	0	0	0	8	2	1	0
Fabless	226	331	49	31	168	80	31

# Patent Portfolio

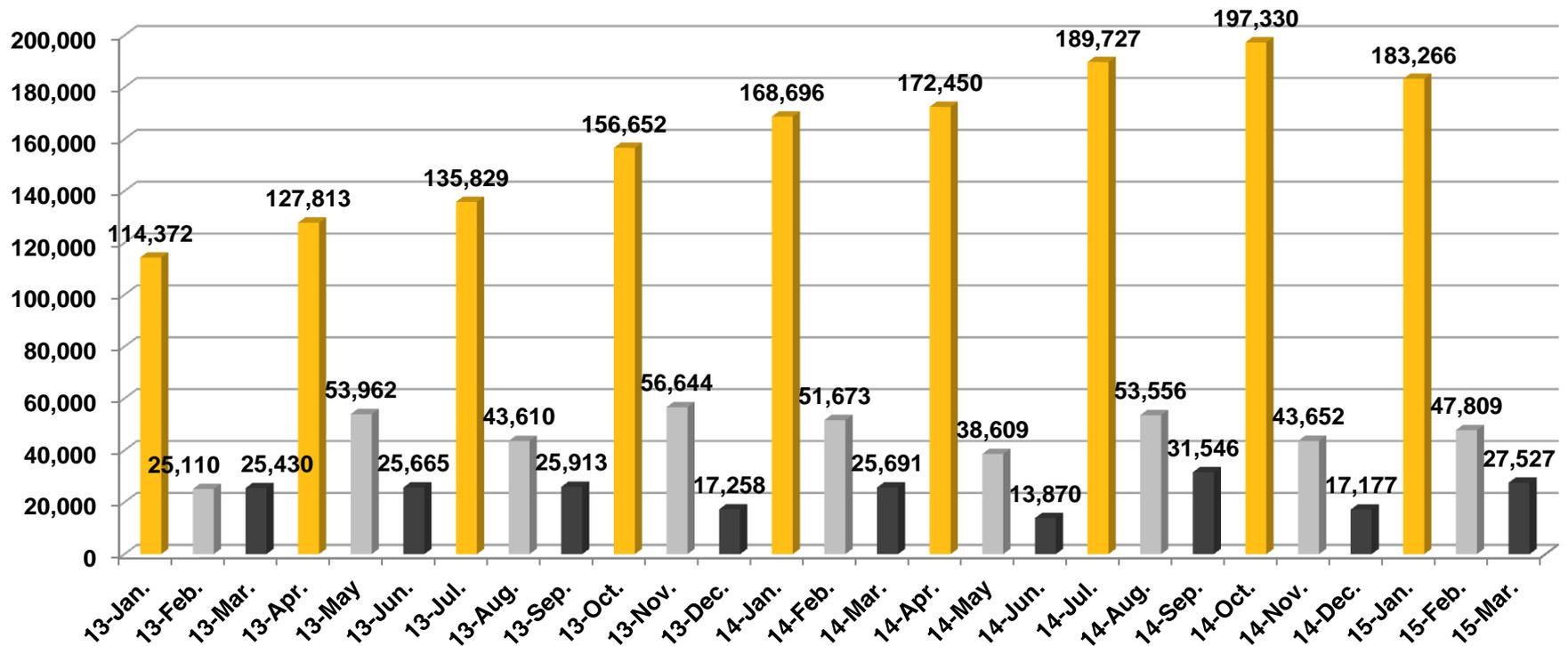
	4Q14	1Q15	Diff.
Pending	166	175	+9
Issued	269	278	+9
<b>Total</b>	<b>435</b>	<b>453</b>	<b>+18</b>



# Quarterly Revenue Pattern

- The quarterly royalty from most of foundries are collected at first month of each quarter and from some other foundries are collected at second month, and none at third month.

Unit : NTD Thousands



# Outline

- **Business Model**
- **Review of Operations**
- **Growth Opportunity and Future Outlook**
- **Q & A**

# 1Q Revenue Breakdown

Unit: NTD thousands

	1Q15	4Q14	% change	1Q14	% change	2014	2013	% change
Licensing	64,056	51,849	23.54%	75,045	-14.64%	246,073	245,688	0.16%
Royalty	194,546	206,310	-5.70%	171,015	13.76%	757,904	562,570	34.72%
Total	258,602	258,159	0.17%	246,060	5.10%	1,003,977	808,258	24.21%

Unit: Number of contracts

		1Q15	4Q14	2014	2013
Technology Licenses		5	3	21	19
Design Licenses	NRE	21	15	82	51
	Usage	82	99	363	342

# Financial Income Statement

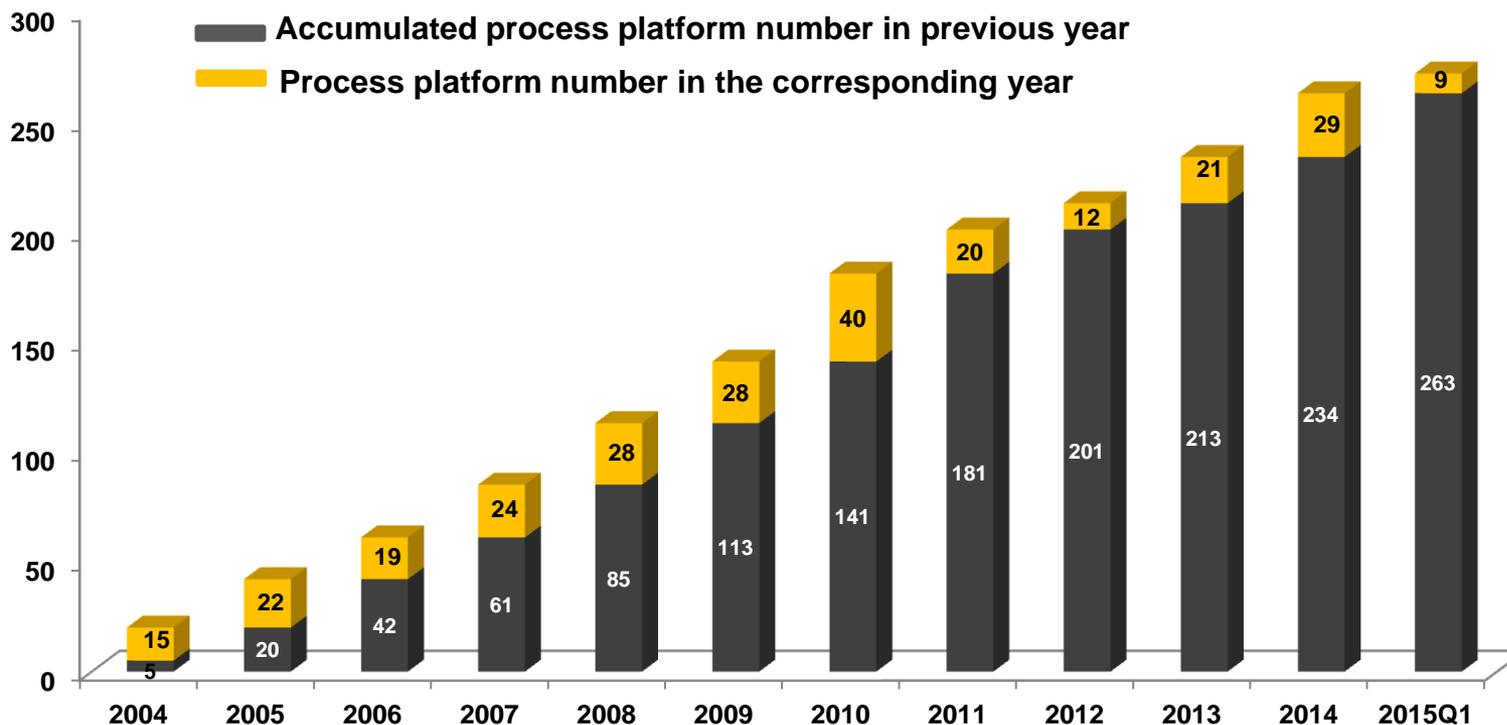
(Unit: NTD thousands)	1Q15	4Q14	% change	1Q14	% change
Revenue	258,602	258,159	0.2%	246,060	5.1%
Gross Margin	100%	100%	-	100%	-
Operating Expenses	128,976	148,501	-13.1%	126,719	1.8%
Operating Margin	50.1%	42.5%	+7.6ppts	48.5%	+1.6ppts
Net Income	114,423	100,896	13.4%	110,936	3.1%
Net Margin	44.2%	39.1%	+5.1ppts	45.1%	-0.9ppts
EPS (Unit: NTD)	1.51	1.33	13.5%	1.46	3.4%
ROE	24.8%	23.4%	+1.4ppts	25.8%	-1.0ppts

# Technology License

Unit: Number of contract

Year	2012	2013	2014	20151Q
License number	12	19	21	5

Note: The terms (including number of process platforms and licensing fees) for each technology license are set contractually. Payments are made according to set milestones, and there are no particular seasonal factors involved.



# Current Technology Development Platforms

- Total (As of Mar.) : **74\***
- **22** for NeoBit, **26** for NeoFuse, **1** for NeoFlash, **17** for NeoEE, and **8** for NeoMTP.

	16nm	28nm	40nm	55/65nm	80/90nm	0.11~ 0.13um	0.15~ 0.18um	>0.25 um	Total
NeoBit	-	-	-	1	-	8	12	2	22
NeoFuse	1	7	4	8	1	3	2	-	26
NeoFlash	-	-	-	1	-	-	-	-	1
NeoEE	-	-	2	-	1	4	9	1	17
NeoMTP	-	-	-	1	2	2	3	-	8

Note\*: 9 platforms qualified in 1Q; 5 platforms kicked off in 1Q.

# Current Technology Development Platforms

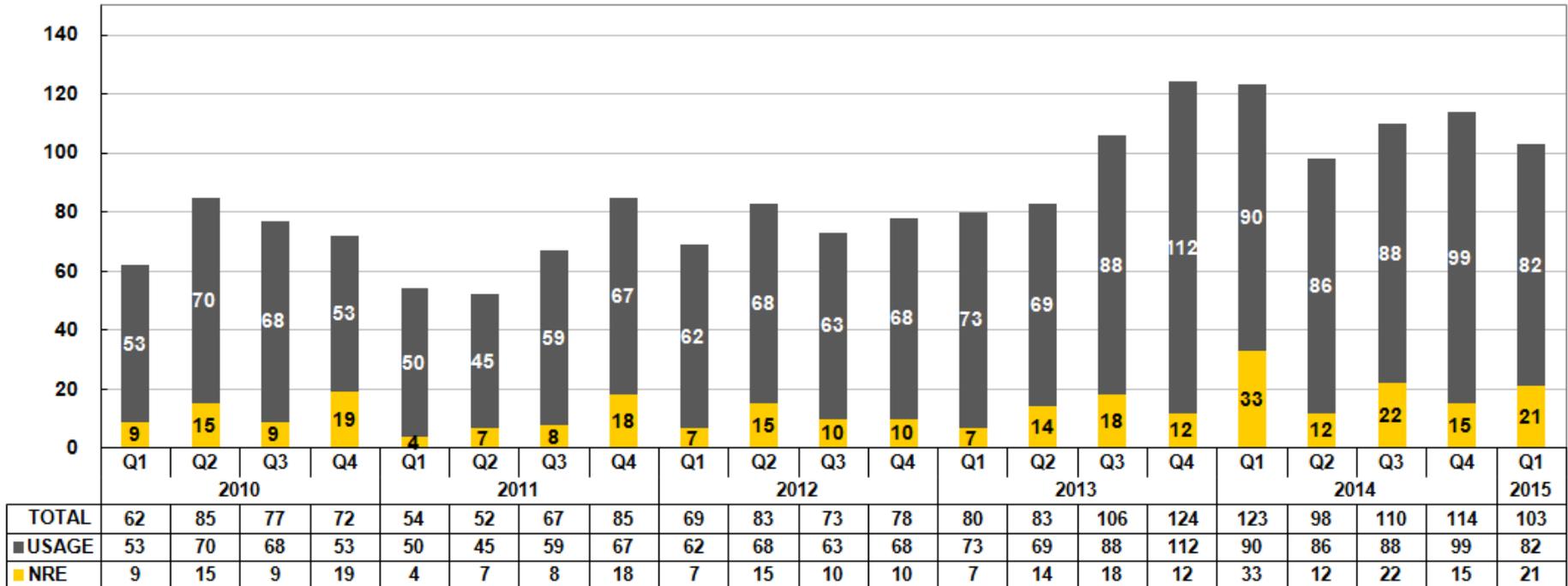
12" Fabs	Production	Development	NVM Type	Process Type
16nm	0	1	OTP	FF+
28nm	2	7	OTP	LP/HPM, HLP/HPM, LPS
40nm	1	6	OTP, MTP	HV-DDI, LP
55/65nm	9	10	OTP, MTP, Flash	LP, HV-DDI, HV-OLED, DRAM, CIS
80/90nm	5	4	OTP, MTP	HV-DDI, HV-OLED, LP
0.13/0.11um	4	5	OTP, Flash	HV-DDI, BCD, Generic
0.18um	1	0	OTP	BCD

8" Fabs	Development	NVM Type	Process Type
0.13/0.11um	12	OTP, MTP, Flash	HV-DDI, BCD, LP, RF, CIS, LL
0.18/0.16/0.152um	26	OTP, MTP	Generic, LP, LL, MR, HV, Green, BCD
0.25um	2	OTP, MTP	BCD
0.35um	1	OTP	UHV

\*As of Mar. 31, 2015

# Quarterly Design Licensing (New Tape Out)

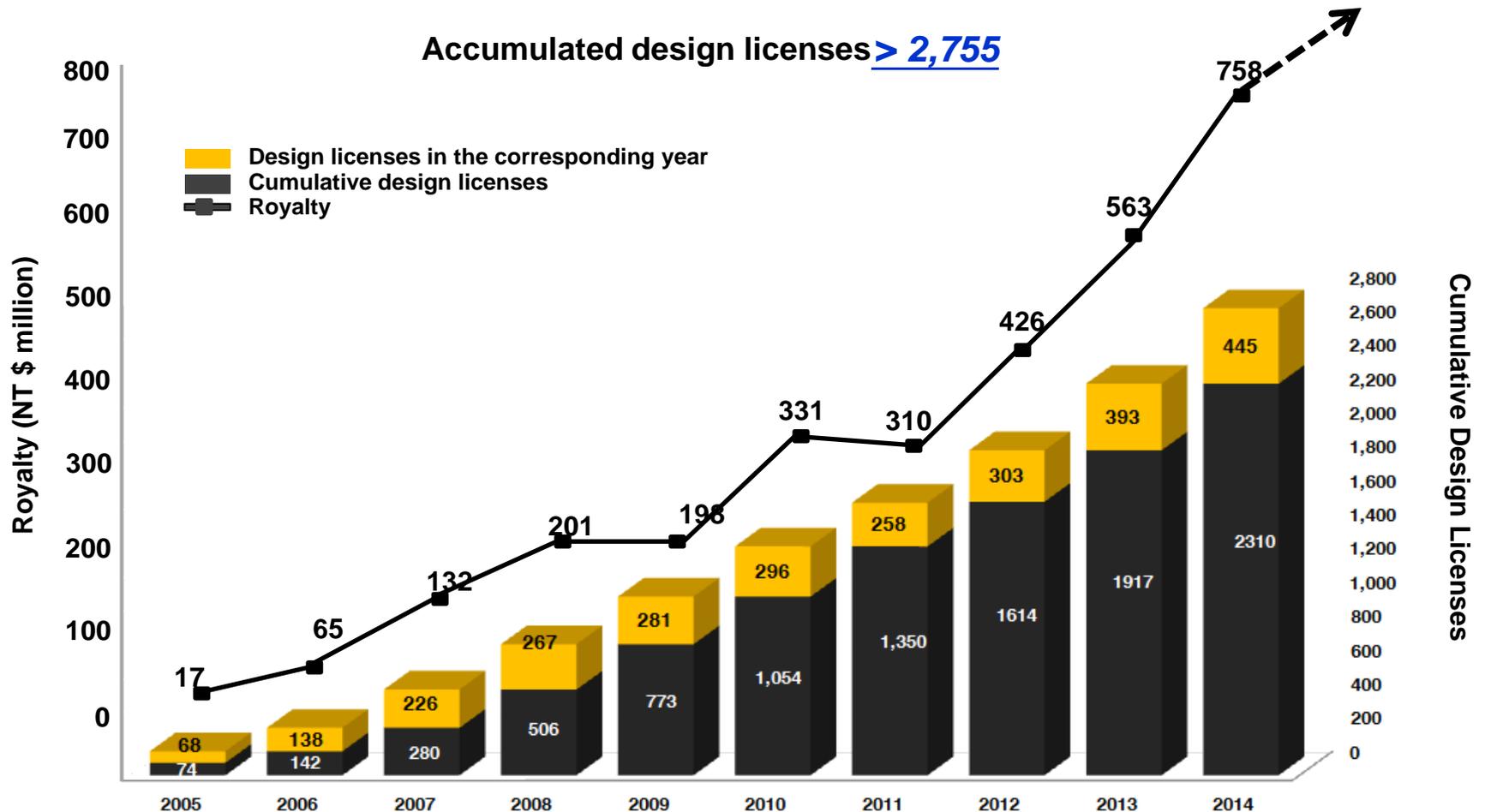
- Total 103 NTO as of 1Q 2015 ( 445@2014 393@2013, 303@2012, 258@2011)



Usage : Usage of pre-qualified and verified IP (charged by per product tape out or annual package), the cycle time from design implementation to royalty payments for mass production is faster, typically less than one year.

NRE: NRE covers the customization of IP that must undergo new verification or qualification. It typically requires 1 to 1.5 years before resulting in royalty revenue.

# Accumulated Licenses Drive Future Royalties

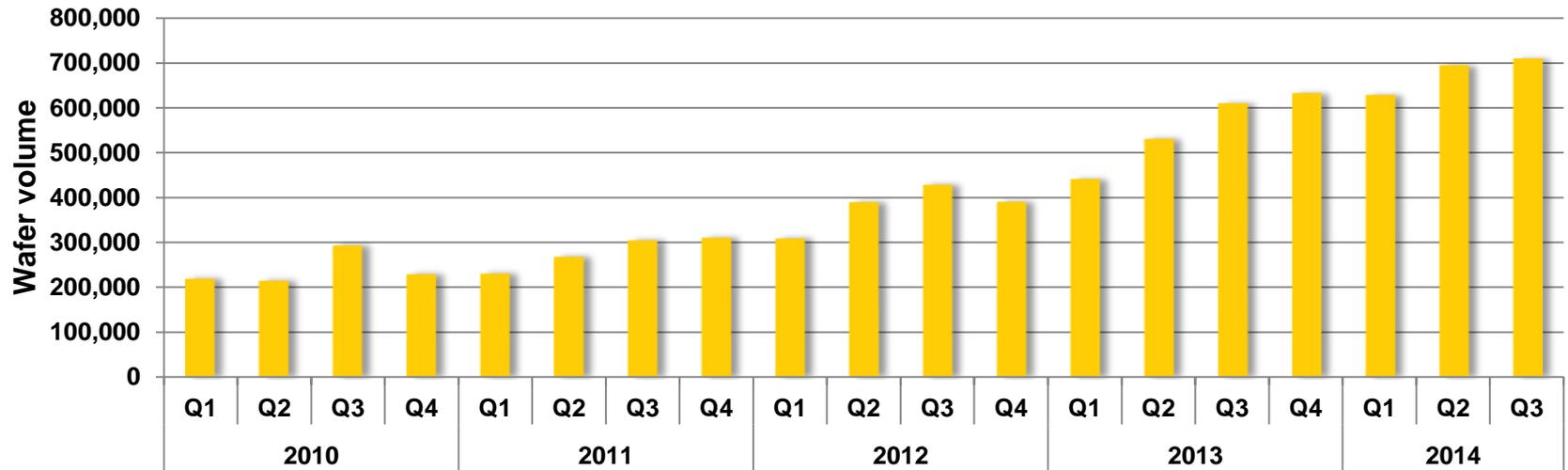


note 1: Due to the 2009 recession, royalty income was down annually 1.5%.

note 2: Pre-payment of royalty fees by a single customer contributed to 2010 annual growth of 67%, causing a drop of 6.3% in the following year, 2011.

note 3: CAGR for 2009-2013 was 30%.

# Wafer Production Volume



embedded eMemory IP in T Company (\$revenue); \* % of Process node in T company total revenue in 4Q14

	Process node	*% of T	4Q14	3Q14	2014	2013
8"	0.5+	1%	0%	0%	0%	0%
	0.25/0.35	4%	30%	33.5%	30.5%	27.3%
	0.15/0.18	12%	8%	13%	11.9%	10.7%
	0.11/0.13	2%	28.9%	21%	20.8%	19.1%
12"	90nm	6%	18.2%	16.4%	16.3%	4.8%
	65nm	11%	0.1%	0%	0%	0%
	40/45nm	13%	0%	0%	0%	0%
	28nm	30%	0%	0%	0%	0%
	20nm	21%	0%	0%	0%	0%
8"		19%	14.2%	17%	15.6%	14.2%
12"		81%	1.4%	1.6%	1.4%	0.69%
<b>Total</b>		100%	4.3%	5.1%	4.5%	4.1%

# Outline

- **Business Model**
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# Applications by Technology

12"			8"					
16/20nm	28nm	40nm	55/65nm	80/90nm	110/130nm	160/180nm	250nm	350nm

**NeoBit**



**NeoFuse**



**NeoFlash**



**NeoEE**



**NeoMTP**



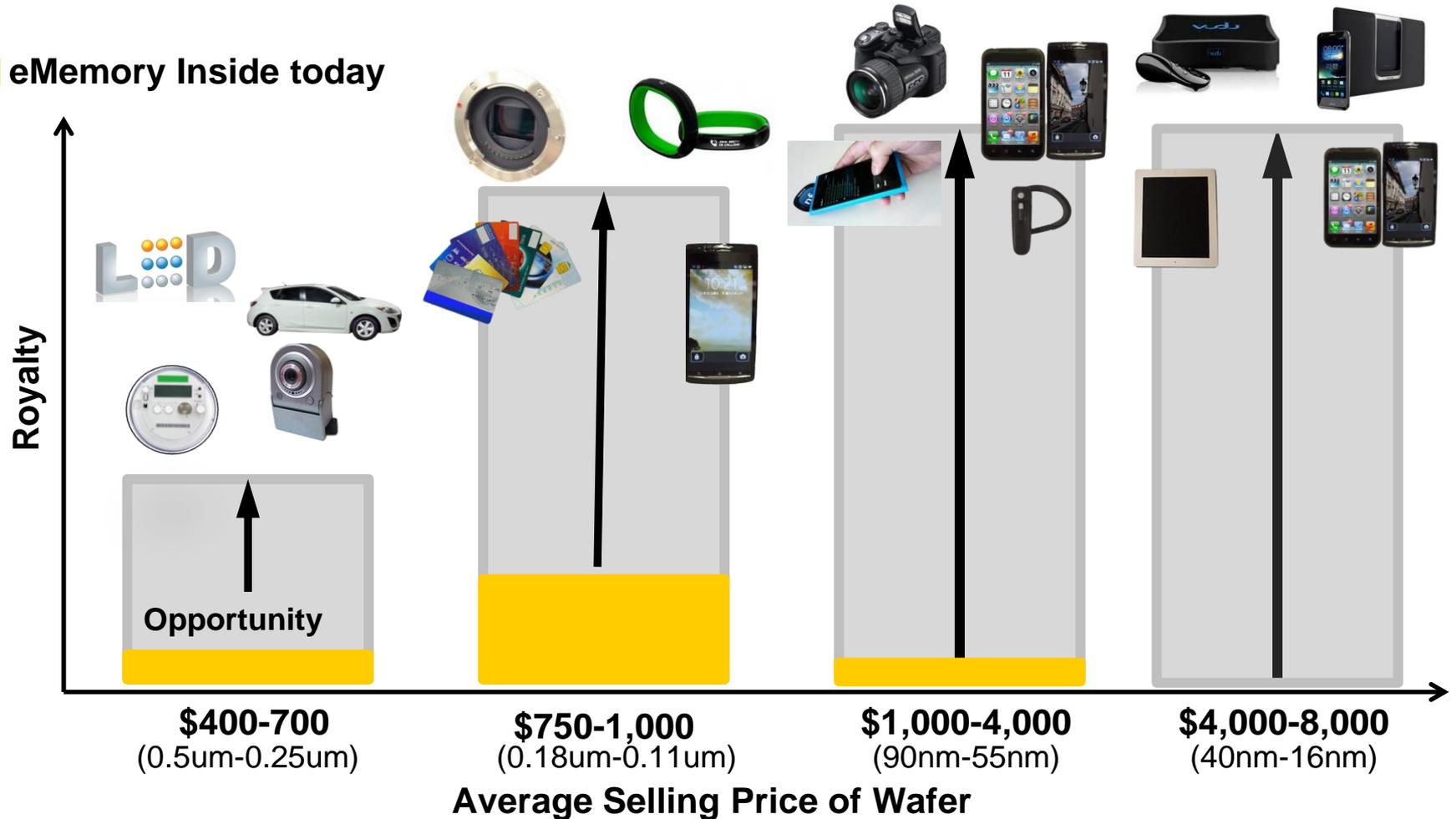
# eMemory's NVM Technologies

- **Logic NVM portfolio offers one-stop-shop solution.**
  - › Compatible to any process
  - › Robust structure
  - › Low process cost
  - › Competitive macro sizes
  - › Easy integration
  - › Easy porting

eMemory's NVM Technology	OTP			MTP	
	NeoBit	NeoFuse	NeoFlash	NeoEE	NeoMTP
Product Type	OTP	OTP	Flash	EEPROM	MTP
Endurance (Cycles)	10	10	1K~10K	10K~100K	1K~10K
Additional Mask Steps	0	0	2-3	0	0
Technology	Floating gate	Anti-Fuse	SONOS	Floating gate	Floating gate
Scalability	Simple	Simple	Simple	Simple	Simple
Memory Density	HD < 512Kb GHD < 16Mb	< 4Mb	< 2Mb	< 4Kb	< 512Kb

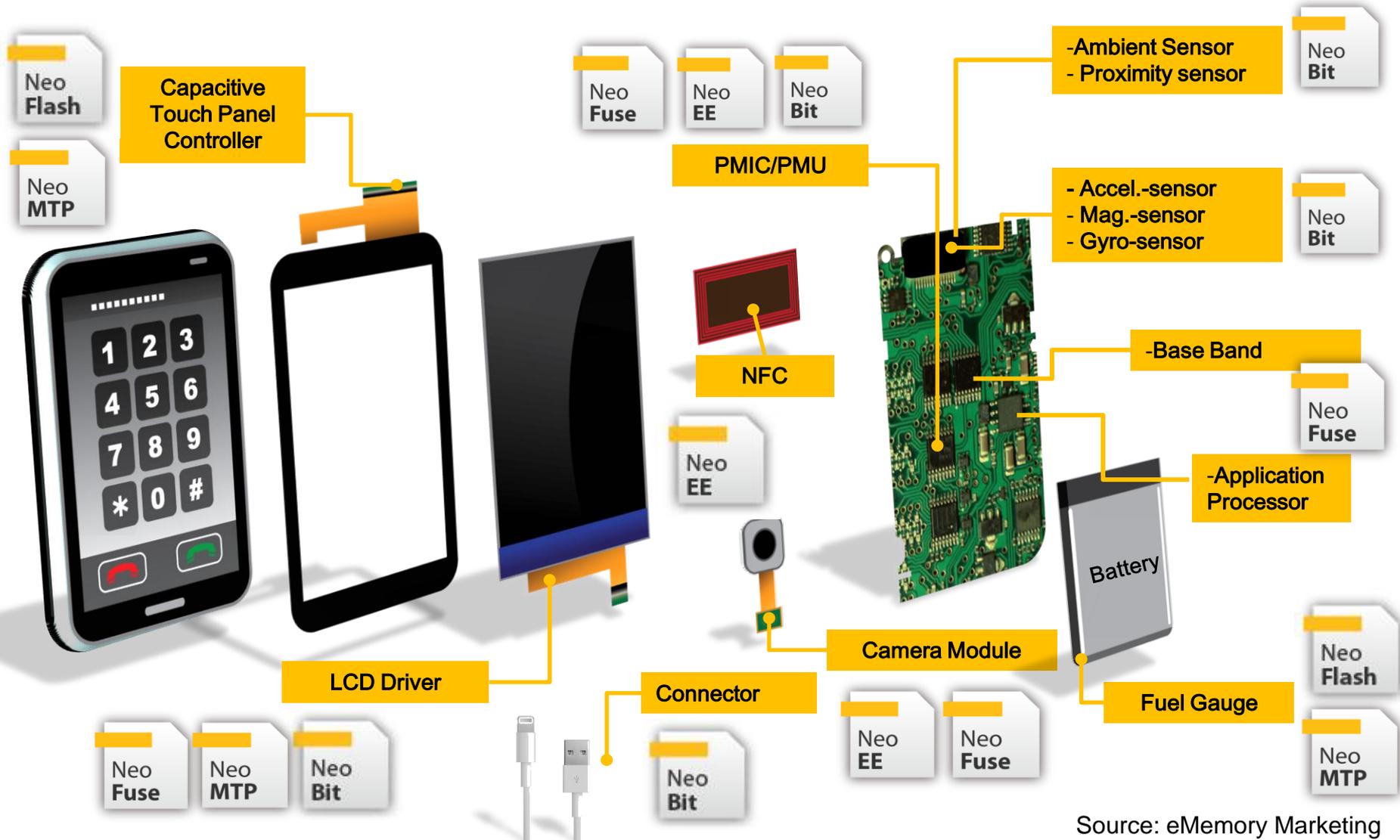
# Opportunity at all Price Points

 eMemory Inside today



Note: 2.2 million 8" equivalent wafers with eMemory IP were shipped in 2013. (~5% of WW foundry shipment)

# eMemory IP in Smart Phone



Source: eMemory Marketing

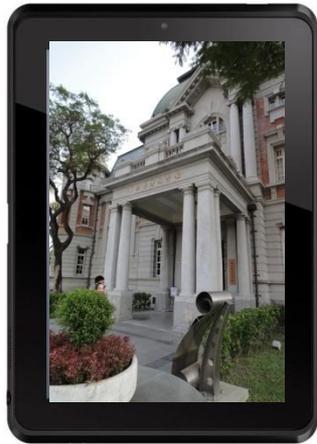
# 3Q14 Wafer Demand by IC Type

IC Type	Equ. to 8-inch wafer (K)
AP	4964
PMU	4756
CIS sensor	4226
Fingerprint	4000
Smart card controller	3000
Base Band	2935
LCD driver ( with TCON)	2013
Gauge IC	627
Touch panel controller ( C )	556
Connectivity	395
STB controller	335
TV controller	327
Wifi controller	245
LED driver	243
DC-DC/AC-DC	176
Accelerator sensor controller	124
Light snesor	121
Bluetooth controller	121
Gyroscope sensor controller	104
TAG IC	76
DVD controller	67
MCU (8bits, LV/3.3V)	56
MCU (8bits, LV/3.3V)	56
P-Gamma	52
MCU (8bits, pure 5V)	51
NB CAM controller	42
Pressure sensor controller	20
Touch pad controller	18
PC CAM controller	15
Touch panel controller ( R )	5
TCON (w/o driver)	4

2014.8.29 updated

# Advanced LCD Driver ICs

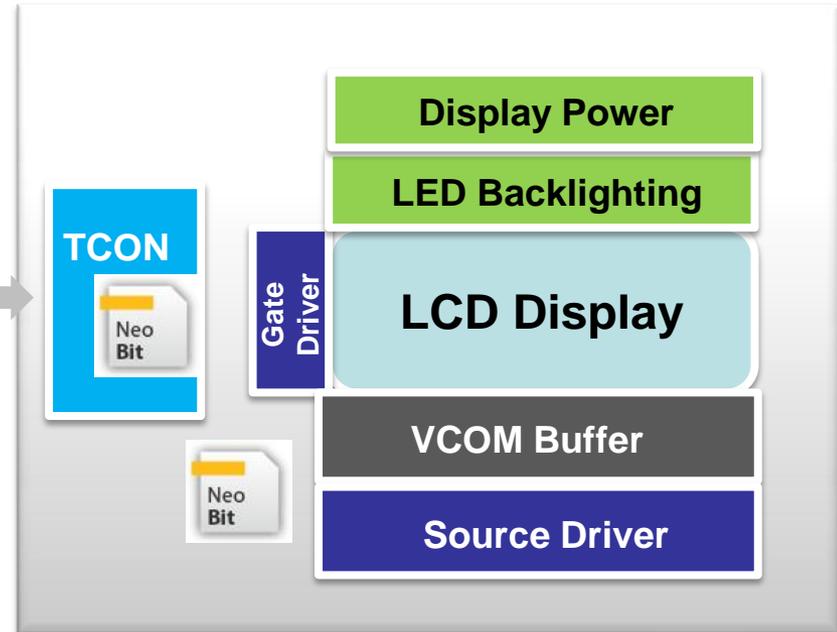
Process Technology : 0.11um HV/80nm HV/55nm HV



I/F  
(LVDS, MIPI,...)



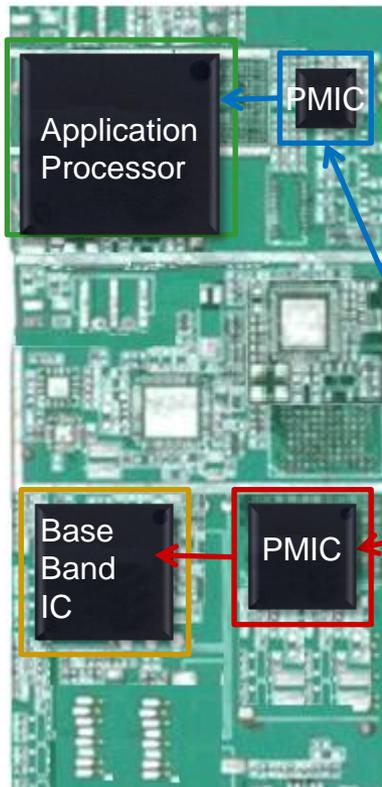
DDI



Density	Endurance	NVM Type	Purpose	NVM Usage
2K8~4K8	1	OTP	Trimming	<ol style="list-style-type: none"> <li>1. Accuracy enhancement</li> <li>2. Mismatch cancellation</li> </ol>
			Code Storage	<ol style="list-style-type: none"> <li>1. Gamma Correction Table</li> <li>2. Timing Control Pattern</li> <li>3. Color Engine Enhancement</li> </ol>

# Power Management ICs for Baseband and Application Processor

Process Technology : Advanced 0.25um BCD/ 0.18um BCD/ 0.13um BCD  
Mature 0.18um/0.16um/0.152um Logic

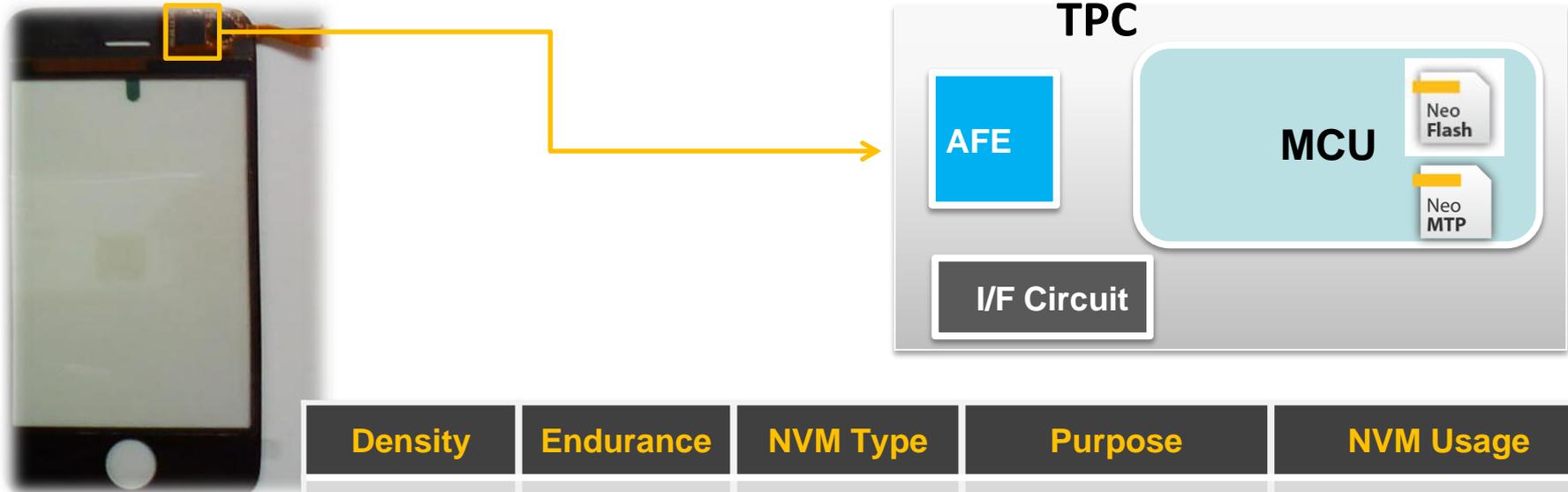


Density	NVM Type	Purpose	NVM Usage
2Kb~4Kb	OTP	Trimming	DC/DC, Bandgap
		Parameter Setting	Design flexibility & Performance optimization
		Code Storage	Start-up behavior & smart power saving algorithm



# Touch Panel Controller ICs

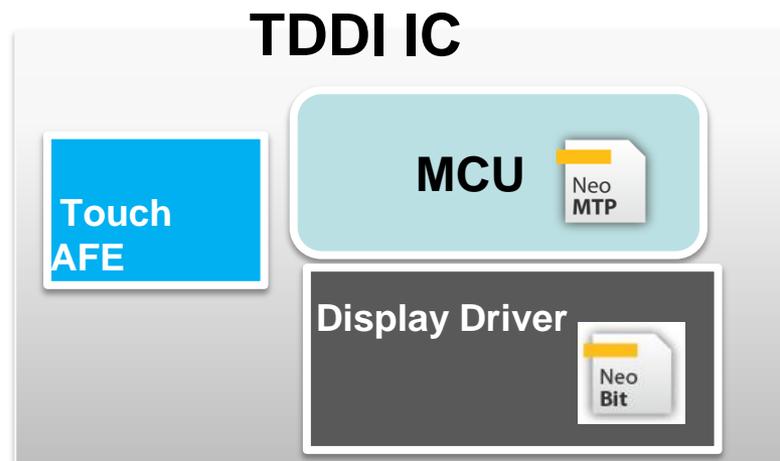
Process Technology : 0.16um HV/0.11um G



Density	Endurance	NVM Type	Purpose	NVM Usage
16K8~32K8	<1000	MTP	Code Storage	F/W code
			Parameter setting	Customized model and performance optimization

# In-Cell Touch Panel Controllers ICs

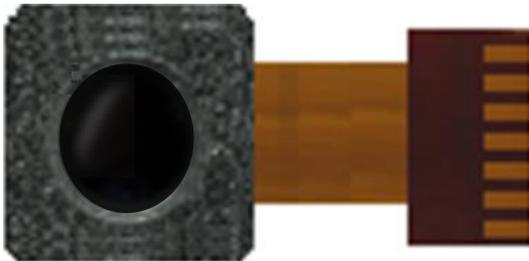
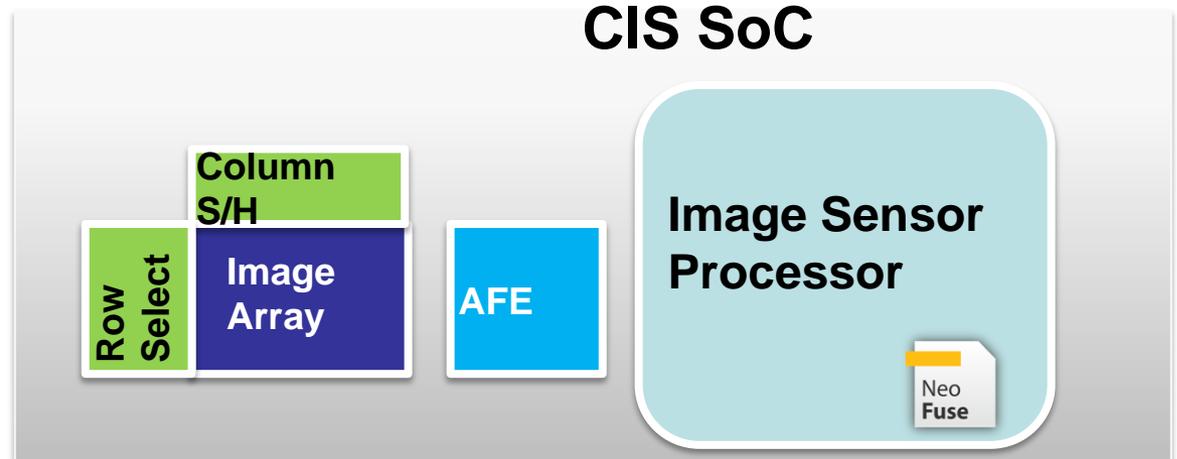
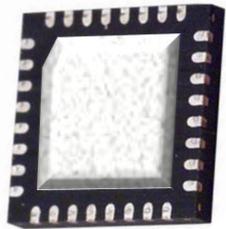
Process Technology : 0.11um HV/80nm HV/55nm HV



Density	Endurance	NVM Type	Purpose	NVM Usage
2K8~4K8	1	OTP	Trimming	Accuracy
			Code Storage	Gamma Table
16K8~32K8	<1000	MTP	Code Storage	Touch F/W Code
			Parameter setting	Performance Optimization

# CMOS Image Sensor

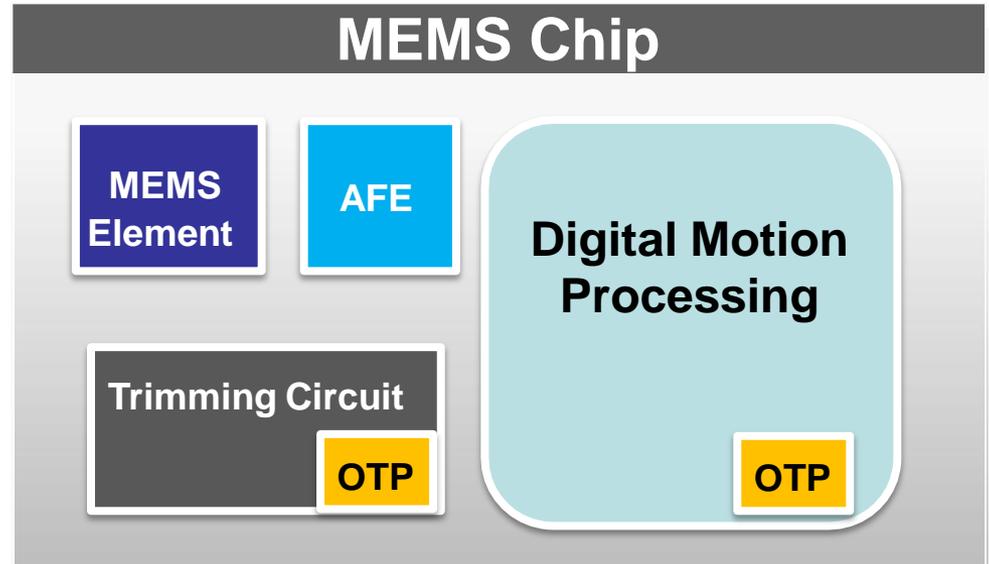
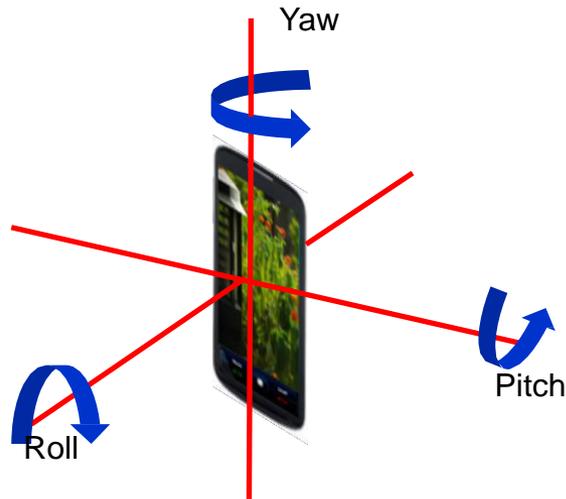
Process Technology : 0.11um CIS/90nm CIS/65nm CIS



Density	Endurance	NVM Type	Purpose	NVM Usage
2Kb~4Kb	1	OTP	Identification Setting	Product Code
			Parameter Setting	Start-up Initial Setting
32K8	1	OTP/ROM	Code Storage	Boot Load

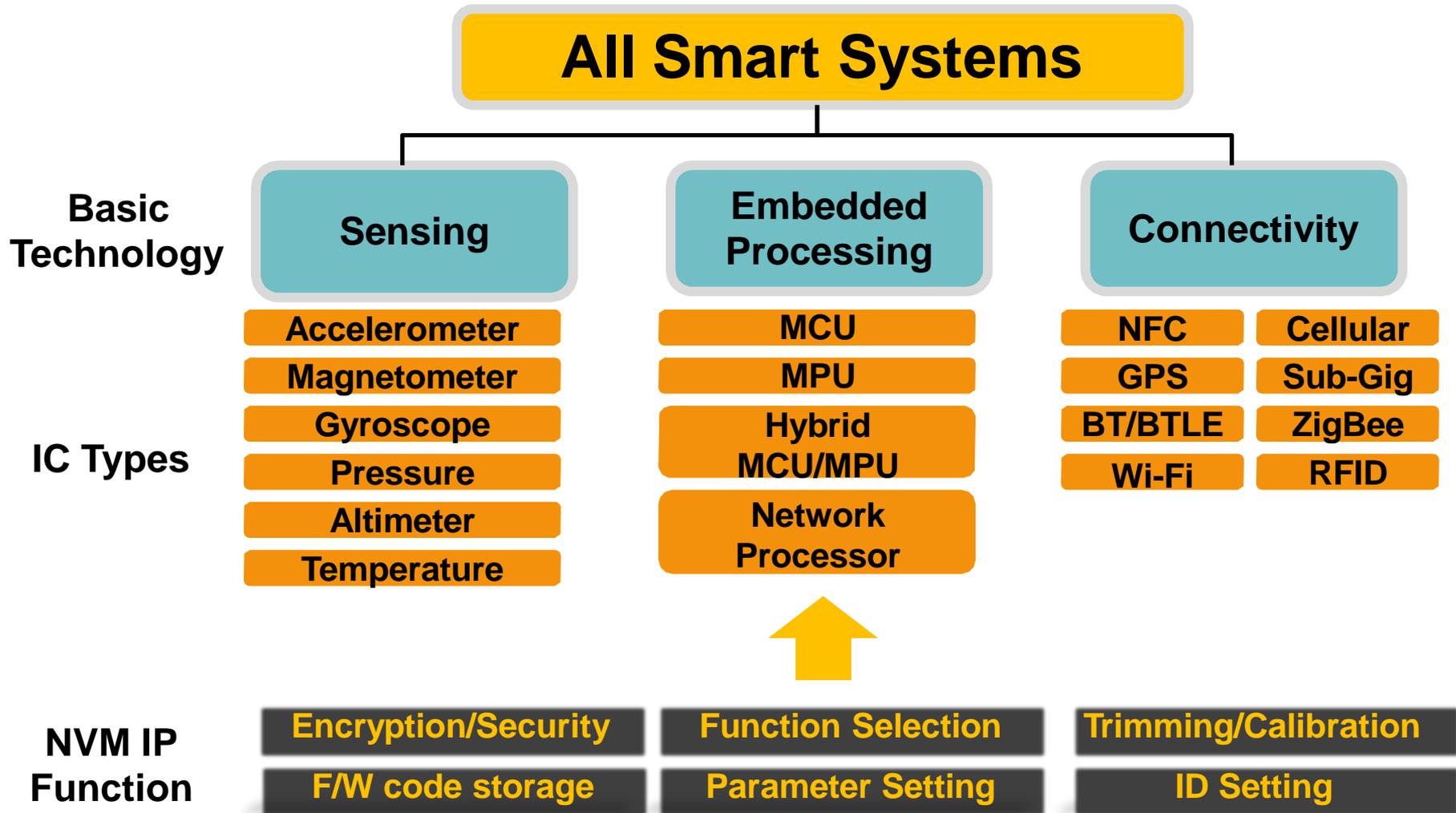
# MEMS

## 180/160/15x nm HV/Logic for MEMS Controller



Density	NVM Type	Purpose	NVM Usage
2Kb~4Kb	OTP	Trimming	Factory trimming
		Parameter Setting	Signal filtering
		Code Storage	Geometric computation

# NVM IP Demand in IoT



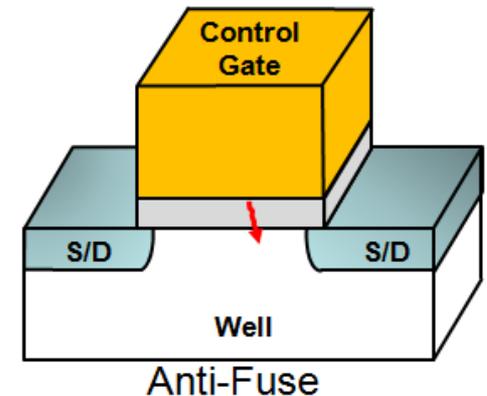
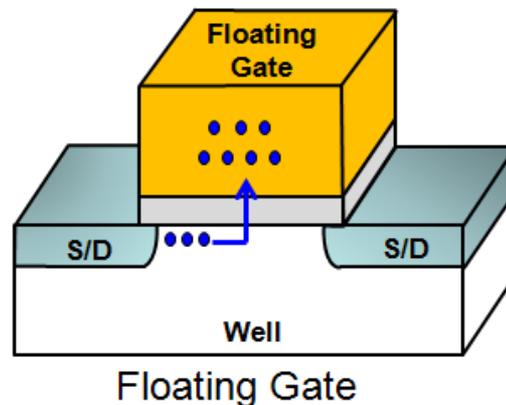
# Invisibility for Security

- Provide “Invisible Hardware Key” for invisible storage
- Prevent reverse-engineering to detect content of security key
- Protect firmware and hardware of ICs from pirating
- Extend & protect customer’s business

eFuse Key: Data is easily observed



Invisible Hardware Key : Data cannot be observed



# Security & Protection

Authorized Product



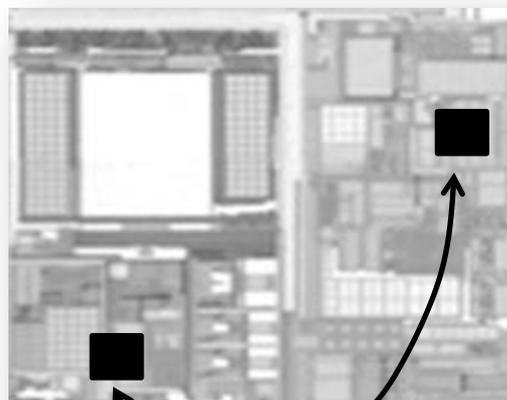
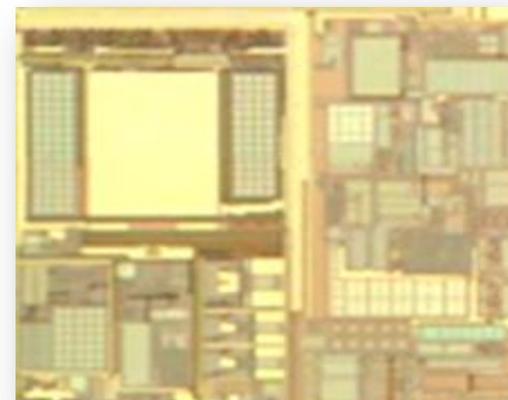
reverse  
copy

re-produce



without protection

Fake Product

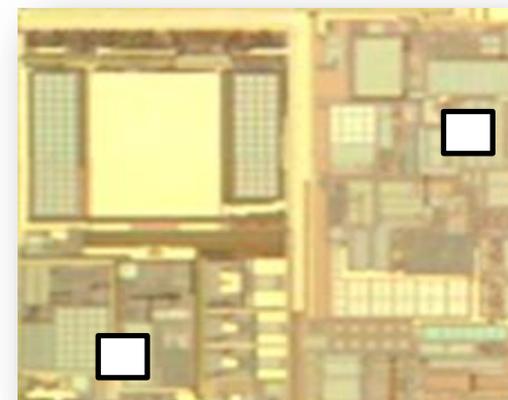


reverse  
copy

re-produce



with protection

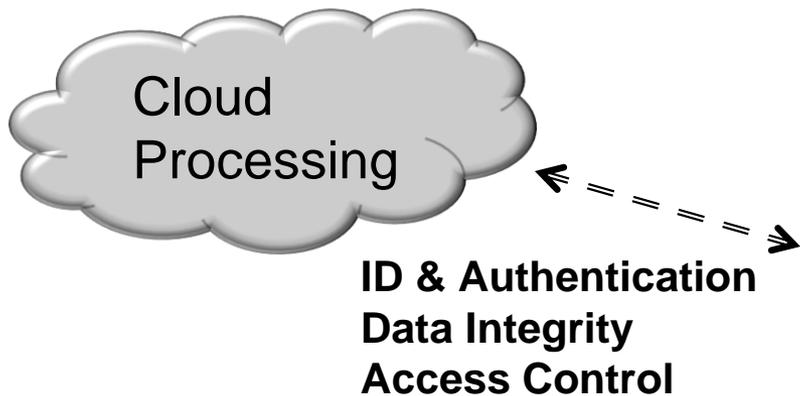


**Security IP/Code by  
Authorized Use**

**Can NOT Work w/o  
Security IP/Code**

# Security with eMemory IPs

## Security for System Service



## Hardware-Software/Firmware Lock



## Hardware Protection Invisible Key for Anti-Cloning

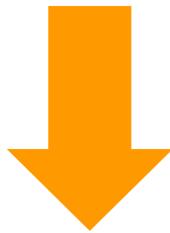


Security IP/Code by  
Authorized Use

# Replacement of Embedded Flash for Competitiveness Improvement

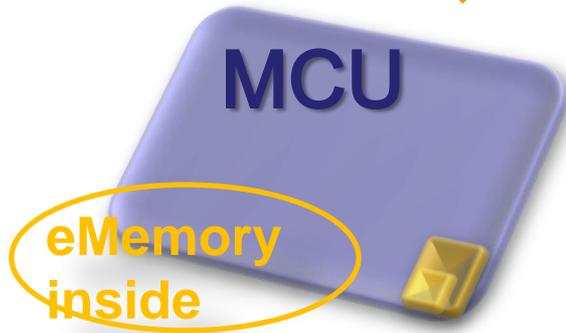


product design & manufacturing by  
embedded Flash  
Logic Process + 10 Masks



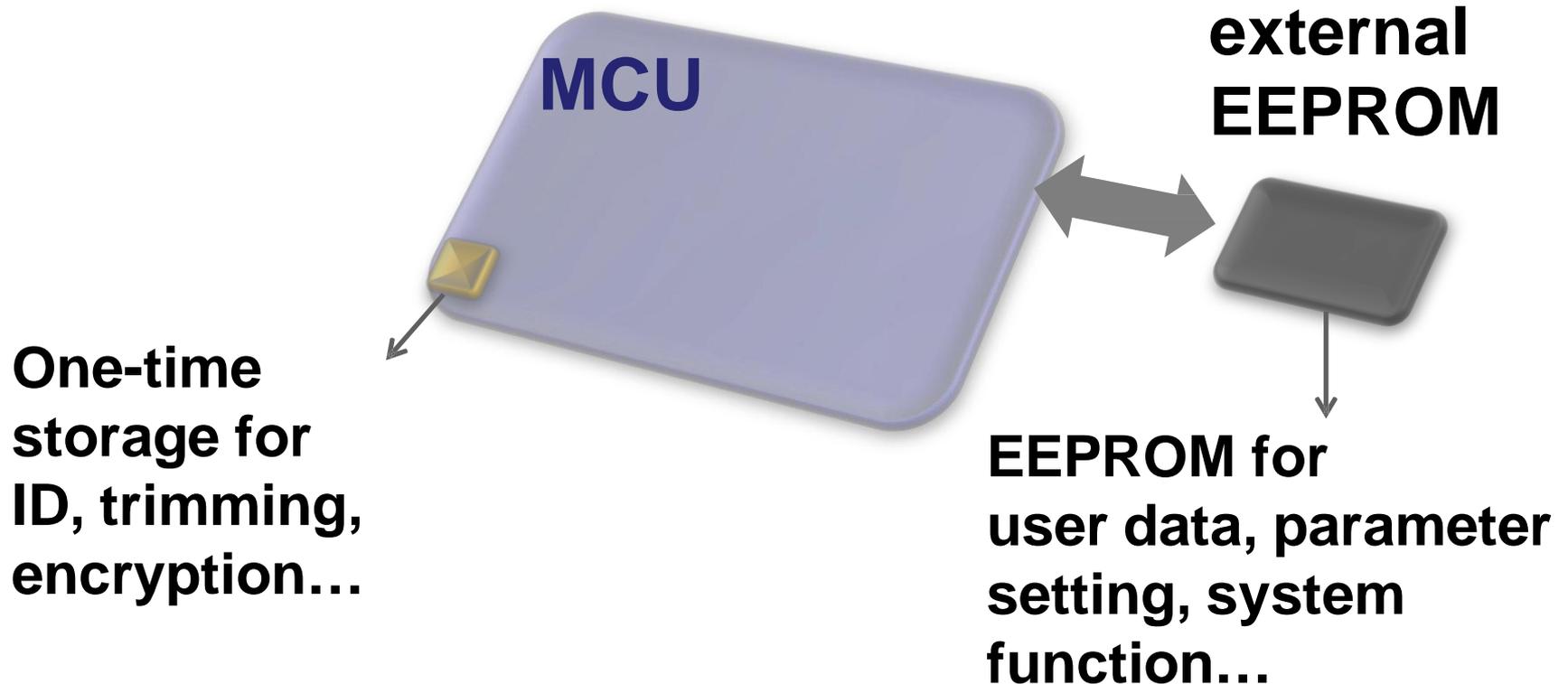
*30% more  
cost reduction*

*wafer cost &  
testing time*



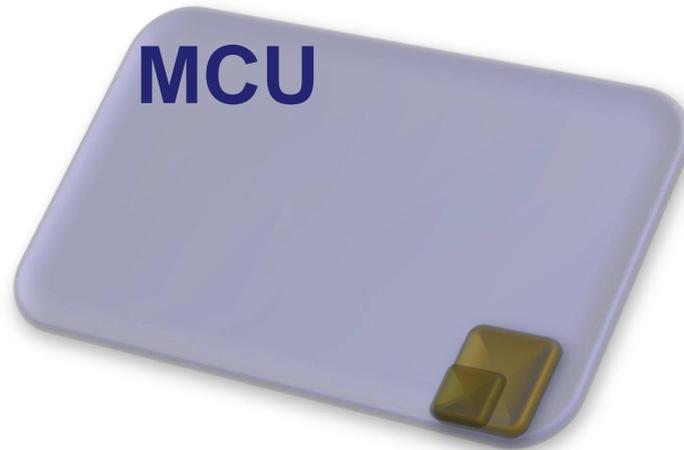
product design & manufacturing by  
Embedded Logic NVM (OTP/MTP)  
Logic Process

# MCU Applications with EEPROM



# NeoBit + NeoEE

Hybrid NVM solution (NeoBit + NeoEE) with  
customized SPEC & optimized size



- One single IP by integration of NeoBit & NeoEE
- Help for system size reduction

# 2015 Outlook

- **Applications in major smart phone customer continue their momentum and expand to wearable devices.**
- **PMICs in Chinese smart phone continue to increase production and expand to new power management applications , such as fast charger and wireless charger.**
- **TDDI and 55nm LCD Drivers start to ramp up.**
- **Applications in STB, Fingerprints, and CIS will ramp up in 2H of 2015.**

# Key Growth Drivers

## Growth in value per mobile devices

- More chip applications per smartphone/tablet product.

## Growth into more markets

- From consumer electronics and mobile devices to wearable devices.
- Adding new NVM product lines further enable more product applications.

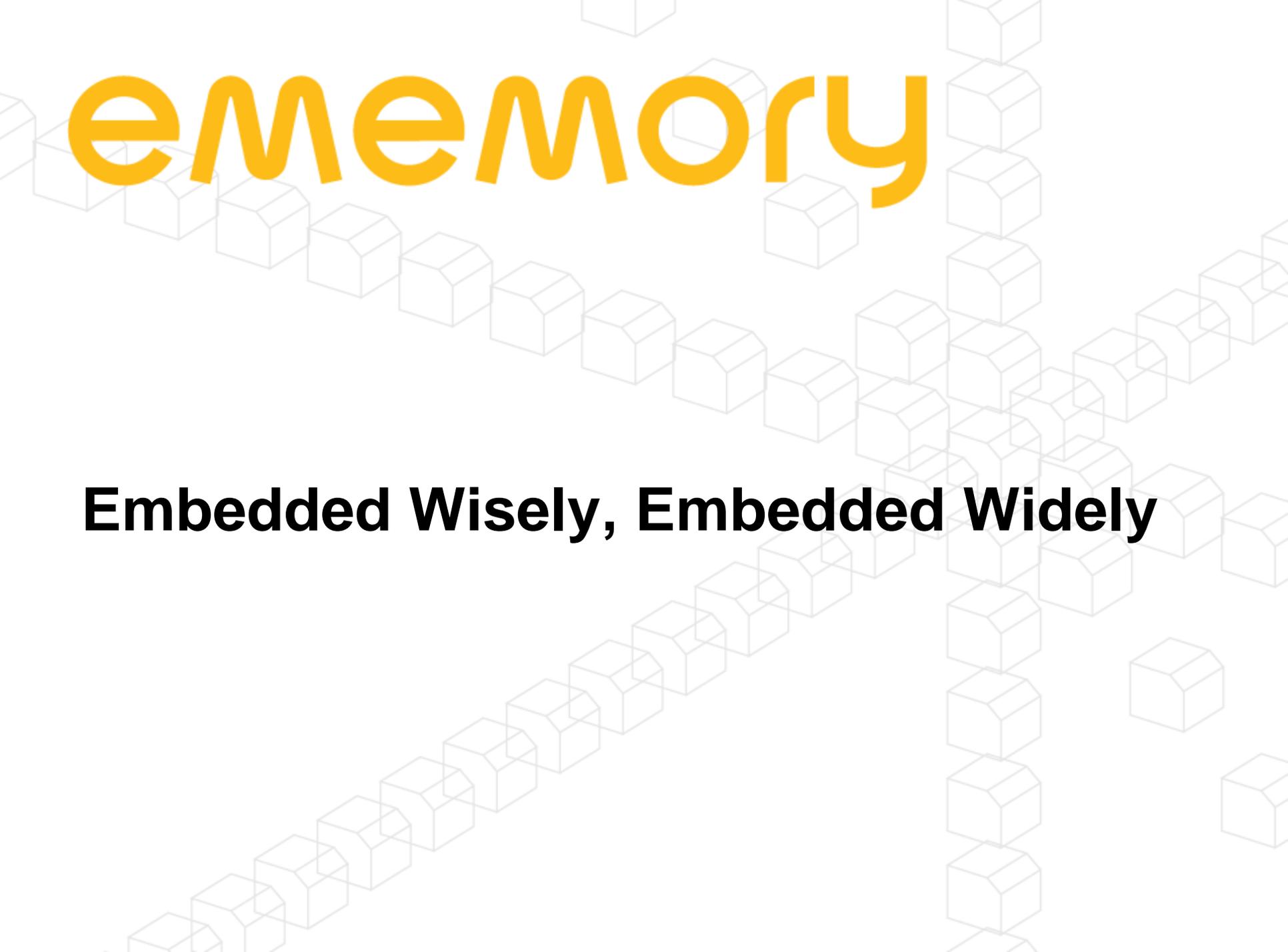
## Growth in more advanced technology

- Higher royalty per wafer is contributed from more advanced technology nodes.

## IoT great era

- Embedded Logic NVM will be a must.

# Q & A

The background of the slide is a light gray pattern of 3D cubes. Some cubes are solid, while others are hollow wireframes. They are arranged in various orientations and positions, creating a sense of depth and a grid-like structure.

# eMemory

**Embedded Wisely, Embedded Widely**