eMemory 1Q26 Earnings Call Q&A Transcript

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Q&A Transcript

1. **Royalty revenue in April declined compared with the previous quarter, while foundry revenues generally increased quarter-over-quarter in Q1. Together with the potential impact from foundry price increases, is there any particular reason for this difference?**

   >>Based on what we have heard, foundry price increases generally start from the second quarter, or are expected to take effect in the second half of the year. Therefore, the impact was not yet reflected in the first quarter royalty.

   The decline in royalty revenue was mainly due to a temporary disruption caused by the sale of one Taiwan-based foundry customer. That foundry happened to be the production site for certain end-customer applications, which led to a short-term decline in royalty contribution.

   We expect this impact to be temporary. As chip customers shift production to other foundries, the related royalty revenue should gradually recover.

2. **What was the reason behind the decline in 8-inch royalty revenue in the first quarter? Will the recent increase in 8-inch foundry pricing provide support going forward?**

   >>The royalty revenue recognized in Q1 reflects foundry shipments from the fourth quarter of last year, and therefore still reflects last year's foundry pricing.

   Since foundry price increases are being implemented gradually this year, the impact on our royalty revenue is expected to be reflected in the second half of the year.

3. **As SRAM becomes increasingly important and density continues to grow, there is a stronger incentive for customers to adopt Repair IP. Could you share the company's development progress in AI-related projects in this area? How many projects are currently in the pipeline, and could we start to see royalty contributions in the coming years?**

   >> Our OTP has long played an important role in SRAM repair applications. We have already worked with Siemens to integrate our technology with its Tessent™ software, offering a validated solution that helps simplify the design process and accelerate customer adoption.

   Currently, the company has multiple AI-related SRAM repair design-ins, mainly focused on advanced-node chips such as AI data center processors, memory controllers, and CXL-related devices.

   As these designs are finalized and move into mass production, we expect the related royalty contribution to become increasingly visible.

4. **Could you provide more details on the development of the company's 1T flash architecture and technology? Can this technology be used for both NOR and multi-level cell, or MLC, applications? Are there any foundries or IC design customers currently engaging with the company?**

>> 1T NeoFlash adopts an innovative write architecture that overcomes the limitations of conventional 2T designs and removes the address selection component. This significantly reduces memory cell area.
Essentially, this is a Flash technology built on standard logic processes. Its key advantages include the ability to support both embedded Flash and standalone Flash, a shorter development cycle, lower cost, higher yield, and greater manufacturing capacity.
We believe this represents a significant innovation, as both embedded and standalone Flash can be more easily implemented using existing logic process platforms. The technology can support NOR Flash, 2D NAND, and multi-level cell, or MLC, applications.
The technology has now entered the active development stage, and we are already collaborating with several foundries and fabless companies.

5. **What are the key differences between embedded memory technology and standalone memory products? Can the know-how we have accumulated in embedded memory be directly applied to standalone memory? Also, who are the potential customers?**
>> eMemory has long built its core technology platform around Logic Non-Volatile Memory, or Logic NVM. This platform helps customers achieve faster development, higher yield, and lower cost across both advanced and mature process nodes.
The key advantages of our technology platform include three areas.
First, **faster development**. Since our technology can be implemented using standard logic processes, it does not require major process changes or modifications to existing device models. This helps significantly shorten the development and adoption cycle.
Second, **higher yield**. Because the technology is fully compatible with standard logic processes and does not require complex special devices or additional critical process steps, it is easier to maintain high yield and stable mass production.
Third, **lower cost**. With a simpler process flow, shorter cycle time, and higher yield, the overall wafer manufacturing and system cost can be effectively reduced.
On our 1T Logic Flash platform, the same core memory technology can support both embedded Flash and standalone Flash. In fact, the core memory array design is quite similar between embedded and standalone Flash. The main difference lies in the system interface.
For embedded Flash, the interface is customized based on the requirements of each SoC system. For standalone Flash, the interface follows industry standards in order to support a wide range of system platforms and end applications.
Therefore, our 1T memory platform can support both embedded and standalone Flash, and also has the potential to extend into both NOR Flash and NAND Flash architectures.
More importantly, because this technology can leverage existing logic process capacity, it does not require customers or partners to build dedicated traditional Flash production lines or make large-scale additional CapEx investments. This gives the technology significant development potential and strategic value, especially as the global Flash supply chain evolves and AI-related demand continues to grow.
Potential applications are broad, including AI servers, Edge AI, smartphones, electric vehicles, industrial control, networking equipment, and various high-security and high-performance computing systems.

6. **Traditional IP companies such as Arm, Rambus, and Alphawave have been expanding into chip products. Is eMemory's move into standalone memory similar? Could this become a future industry trend?**

>> The companies mentioned are mainly IP design companies. They typically develop IP products based on existing process technologies and standard transistor architectures. eMemory's core competitiveness, however, lies in the invention and platformization of memory technology itself.

We are not only designing IP. We innovate from the underlying memory device, process integration, and architecture level to build a complete technology platform. As a result, in addition to developing and selling IP ourselves, we can also license our core memory technologies to other companies, allowing partners to further develop them into IP or end products.

From a business model perspective, we will continue to operate our IP business directly in order to maintain technology leadership and market influence. On the product side, we can enable more partners to participate in productization and mass production through technology licensing, while eMemory collects royalties based on product shipments.

Since product licensing is closer to the end market in the value chain, the potential royalty scale is typically much larger than that of traditional IP licensing.

This has always been an important growth direction for eMemory: to evolve into a technology licensing company with a strong core technology platform and broader influence across the product ecosystem.

7. **What are the key drivers of revenue growth this year?**

>> Revenue growth this year is driven by both upgrades of existing applications and the ramp-up of new applications.

For existing applications, product upgrades have led to higher royalty ASPs, such as OLED DDI for foldable smartphones at 16nm, and PMIC migration from 8-inch processes to 55nm. At the same time, several new applications are gradually entering mass production, including smartphone modem-related chips, AI CPUs, BMCs, embedded controllers, SSD controllers, CXL controllers, DIMMs, and high-speed networking interface applications. These new ramps are expected to further support revenue growth.

8. **As mature-node foundries raise prices while consumer smartphone demand remains weak, how does the company view the effectiveness and sustainability of these price increases?**

>> We believe mature-node price adjustments are supported by structural factors.

First, leading foundries are allocating more resources to the most advanced process nodes and advanced packaging. This indirectly reduces the effective capacity available for mature nodes.

Second, AI-related applications still require a significant amount of mature-node capacity, whether in data centers, edge AI, or physical AI. Many supporting components, such as high-voltage and high-current power devices, are still manufactured on mature nodes.

A good example is the recent development of Co-Packaged Optics, or CPO. In a CPO architecture, usually only the most critical components, such as switch ASICs or DSPs, adopt advanced nodes like 5nm or 3nm for maximum computing efficiency. Many surrounding optical, analog, and power-related components continue to use mature nodes to achieve the best balance of performance, power, area, and cost.

We have also observed that some foundry customers are reallocating capacity and resources. For example, certain power-related businesses are being shifted to other foundry partners, while more resources are being directed toward developing CPO-related processes.

9. **With the continued advancement of advanced nodes and growing demand for high-performance computing, are you seeing more adoption opportunities for your solutions on Arm-based platforms?**
   >> As AGI CPUs move into mass production, demand for Root of Trust, or RoT, solutions among advanced-node CSS customers has increased significantly. We have already seen multiple customers adopt related solutions.

10. **Could you share the progress of the company's collaboration with Intel Foundry?**
    >> Our collaboration with Intel Foundry is mainly focused on advanced-node OTP and PUF-based security IP.
    We are actively working to bring our PUF-based IP onto Intel 18A to address supply chain security requirements from the U.S. government and related markets.

11. **What is the potential from DRAM module-related applications? Which product lines would benefit the most?**
    >> DRAM module-related applications represent an important growth opportunity for our OTP, MTP, and Security IP businesses.
    This is mainly driven by AI servers, which are increasing demand for DDR5, CXL memory, HBM, and high-speed memory modules. These products require stronger yield management, module configuration, and security protection.
    For **OTP**, the main applications are repair and identification, such as memory repair.
    For **MTP**, the main applications are updatable configuration and module management, such as SPD Hub and PMIC settings in DDR5 DIMMs.
    For **Security IP**, the main applications are data security and hardware root of trust. Going forward, DRAM modules will no longer be viewed simply as memory components. They will become key nodes in AI servers, CXL memory pools, and data center architectures. As a result, security requirements will continue to increase.

12. **As the company expands into more technologies, will this require significant R&D investment and lead to a sharp increase in operating expenses?**
    >> Most of our technologies are built on years of accumulated know-how and are extensions of our existing core technology platforms.
    Our technologies are ultimately implemented by foundries and chip companies. Under our business model, partners pay licensing fees that help cover the cost of our R&D teams. In addition, capital expenditures during the development process, such as test chips and related equipment, are typically borne by customers.
    This has been our long-standing business model. It also reflects the strength of our core technology and the significant value our technologies bring to customers. Otherwise, this model would not be sustainable.

For the technologies we are currently expanding into, much of the core R&D and patent development has already been completed. Going forward, the additional expenses will mainly come from execution-related R&D headcount.

As licensing projects increase, the related licensing revenue should be sufficient to support the required R&D investment. Therefore, we believe operating expenses will remain within a manageable range.

13. What is the company's progress in next-generation AI computing platforms, such as the Vera Rubin AI platform?

>> The Vera Rubin platform is the first computing generation to adopt Caliptra 1.0, which was released by the Open Compute Project, or OCP, in March 2024. This is also the first specification to include OTP and PUF in the design requirements.

Based on this specification, our technologies have started to be adopted in CPUs, BMCs, SSD controllers, CXL controllers, and networking-related chips. Importantly, OCP specifications are not limited to the Vera Rubin architecture. They are also applicable to cloud service providers, telecom operators, and large enterprises building private cloud data centers.

After that, OCP further released Caliptra 2.0, which includes PQC, as well as the Foundation Chiplet System Architecture, or FCSA, mentioned by our chairman earlier in this earnings call. FCSA clearly requires every chip in a chiplet system to include a Hardware Root of Trust. This reflects the market's growing need for a unified hardware security architecture and persistent data management.

Under this trend, functions such as chip repair, data storage, and hardware root of trust are gradually being adopted across different computing components, moving toward a more consistent architecture. As each new generation of AI platforms evolves, we expect our penetration in AI-related applications to continue expanding over time.

14. As the company expands its security business toward system-level solutions, what would the business model look like? Who are the potential customers?

>> In the development of hardware security systems, our core strategy has two main directions.

First, we are using PUF as the core foundational technology to develop next-generation Hardware Security Modules, or HSMs.

Second, we plan to use HSM as a security platform to further develop Security as a Service, or SECaaS, applications and services.

Through this architecture, customers will be able to build hardware security systems with a high level of security and trust. These systems can protect not only the operation of devices and systems themselves, but also broader application-layer security needs, including AI, communications, data protection, identity authentication, and cloud services.

In terms of business model, eMemory will continue to focus on technology licensing. We plan to license the HSM platform and related security technologies to OEMs and system companies for productization and mass production, and collect royalties based on end-product sales.

Potential customers include telecom operators, hardware security equipment providers, Edge AI OEMs, industrial PC companies, AI infrastructure providers, and various AI and cloud system operators that will have growing demand for post-quantum cryptography, or PQC, and hardware Root of Trust.

15. What is the company's progress in system-level hardware security? How should we think about future HSM or Security as a Service opportunities?

>>The company's development in hardware security is gradually expanding from our existing IP licensing business into system-level security solutions.

Overall, we can look at the architecture in three layers: the HSM core computing layer at the bottom, the key and certificate management layer in the middle, and the application service layer on top.

At the **HSM core computing layer**, we are using PUF technology as the foundation for hardware root of trust. Based on this foundation, we are developing different types of HSM products to support personal devices, compliance needs for small and medium-sized enterprises, and high-end network HSM applications. Going forward, these products will further integrate Post-Quantum Cryptography, or PQC, and PUF technologies, with the goal of meeting international cybersecurity certification requirements. This will help strengthen product credibility and market acceptance in high-security applications.

At the **key and certificate management layer**, we are also working with external certificate and PKI ecosystem partners. The goal is to integrate our underlying hardware security capabilities with certificate management systems, and provide a more complete "HSM + PKI" solution. This will help customers adopt hardware-based security architectures more efficiently for identity authentication, key management, digital signatures, and system trust management.

At the **application service layer**, we have completed the development of our Signing as a Service platform. In the future, this platform can support applications such as digital signatures, device identity, trusted data verification, and DID Wallets. This means the company can not only provide hardware security IP, but also has the opportunity to participate in Security as a Service business models.

To conclude these things, overall, HSM and Security as a Service represent an important direction for the company as we expand from an IP provider into a system-level security solution provider. In the near term, our focus remains on technology integration and application validation. Over the medium to long term, we see opportunities to build new business models and growth drivers through HSM platform licensing, PKI integration solutions, and upper-layer security services.